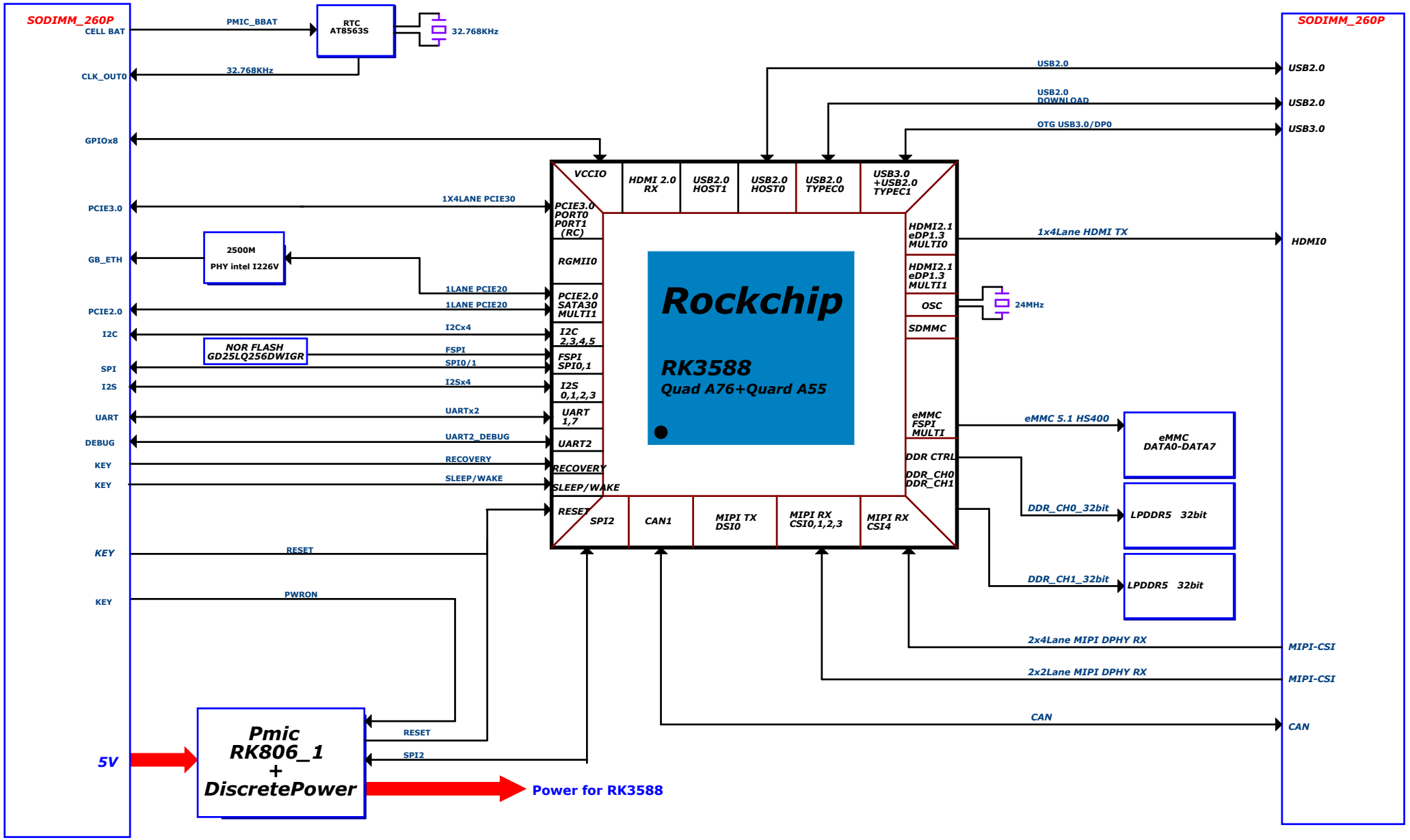
Revision History

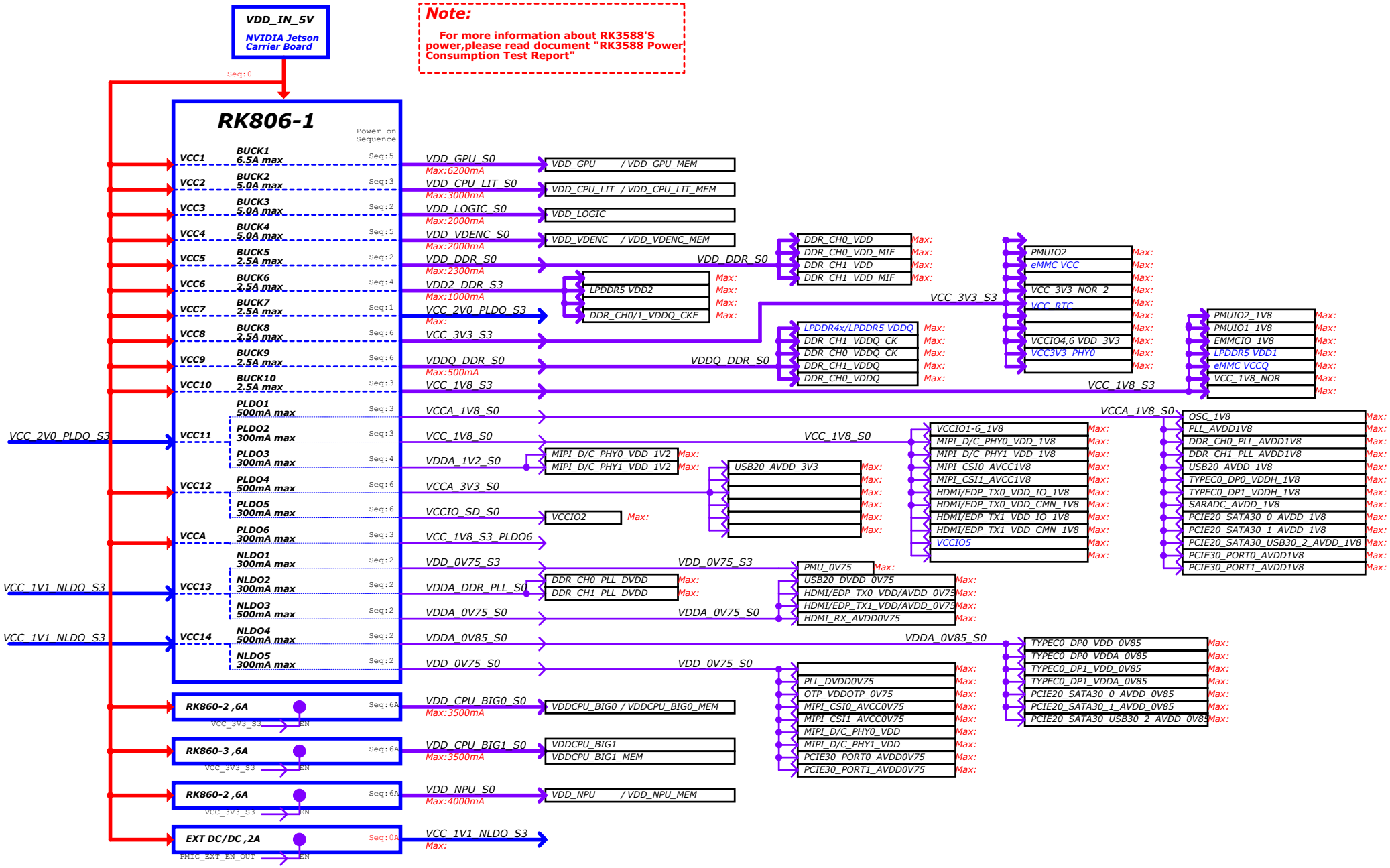
Version	Date	By	Change Description	Approved
V1.0.0	2023-7-21	LOWELL	1:Revision preliminary version	Shawn
V1.1.0	2023-9-21	Shawn	1:Added Matching Circuitry to the Clock Signal of the PCIE Clock Chip 2:Modified Peripheral Configuration Resistors for PCIE Clock Chips 3:Corrected the resistance value of the UART interface	Shawn
V2.0.0	2025-12-01	Sommer	1:Two LPDDR4 chips have been replaced by two LPDDR5 chips 2:Add SPI-NOR-Flash for fast U-boot startup 3:Change MIPI-CSI to two 4-Lane and two 2-Lane. 4:Replace the 1000M Ethernet PHY with a 2500M Ethernet PHY 5:Add a second PCIe 2.0 lane 6:Change DP0 to DP and implement USB multiplexing function	Shawn
V2.1.0	2026-06-03	Sommer	1:Update the PCB outline. 2:Compatibility has been implemented for the MODULE_ID I/O. 3:CSI0 and CSI1 have been swapped at the SODIMM_260pin connector.	Shawn

Revision History



FOCAL CREST 致趣	Design Name: CORE3588E_V2.1.0	
Size: A2	Page Name: 02.Block Diagram	Rev: V2.1.0
Date:	Sheet 2 of 20	

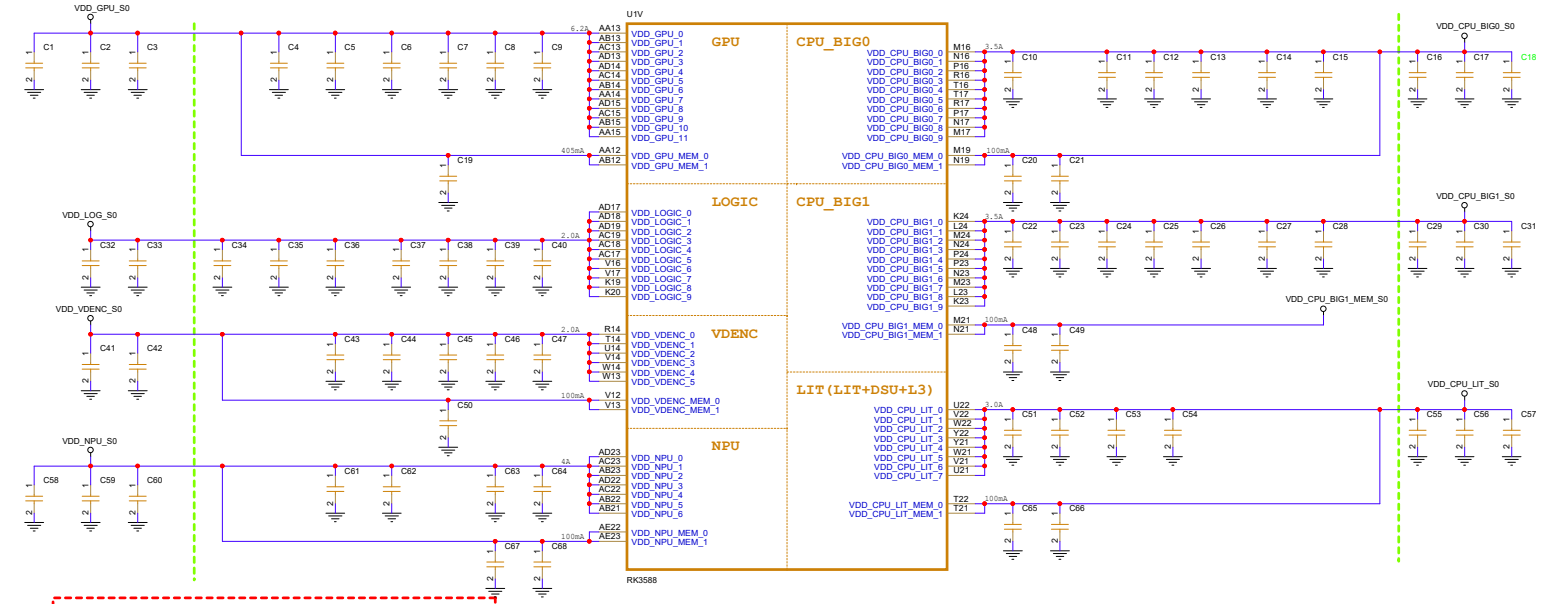
Power Tree



FOCAL CREST 致趣

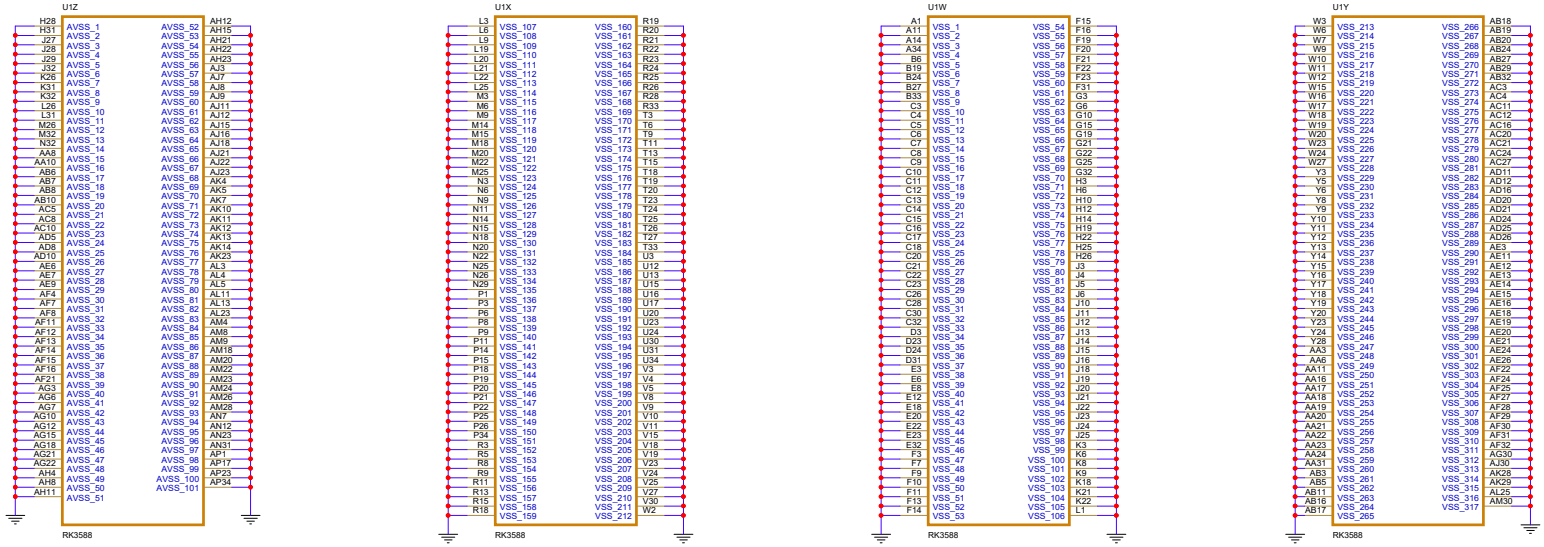
Design Name	CORE3588E_V2.1.0
Size	A2
Page Name	03.Power tree
Rev	V2.1.0
Date:	
Sheet	3 of 20

RK3588_V(POWER)



Note:

The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



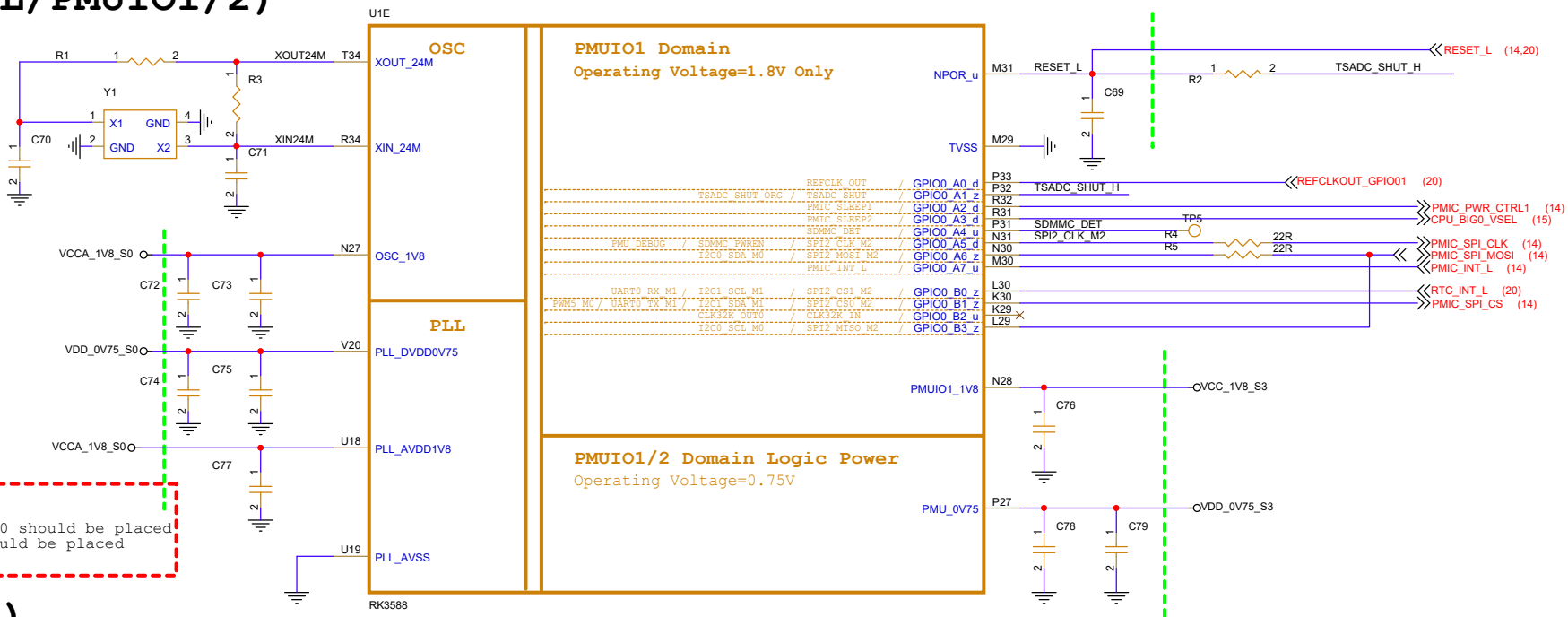
Design Name	CORE3588E_V2.1.0		
Size	Page Name	Rev	
A2	04.RK3588_Power/GND	V2.1.0	
Date:	Sheet 4 of 20		

RK3588_E(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification

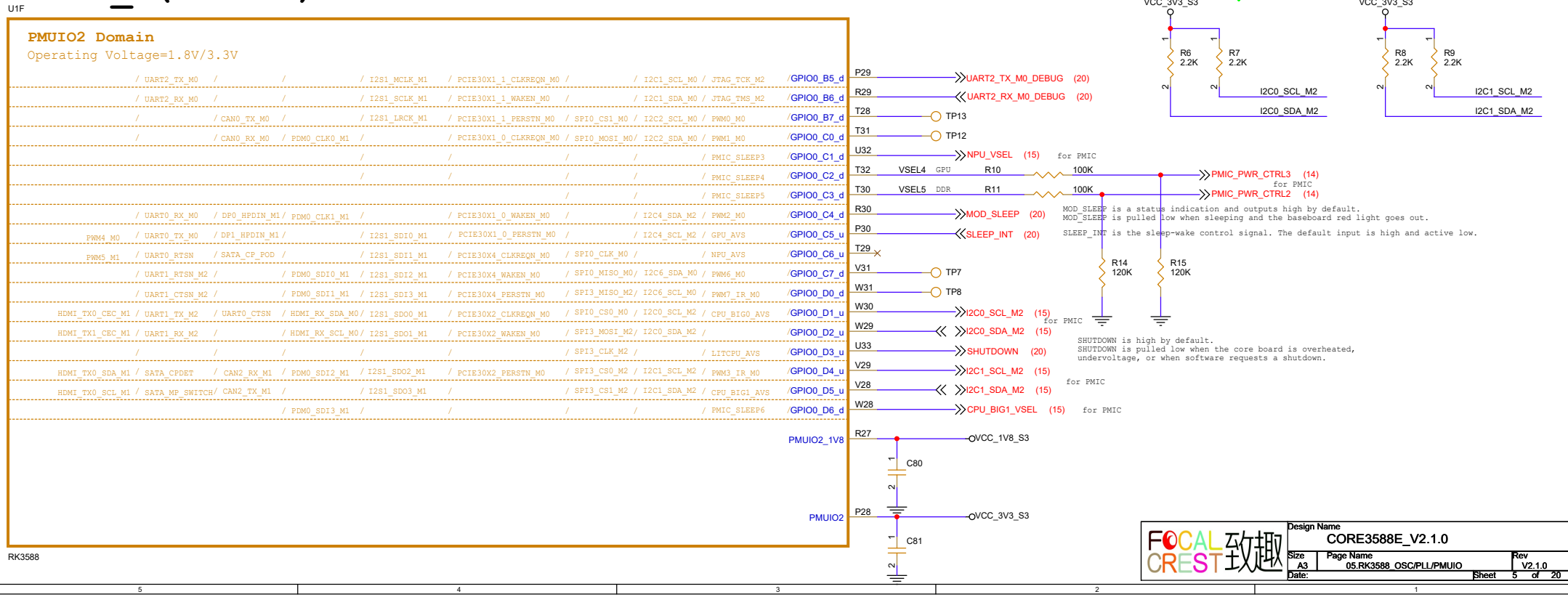
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF

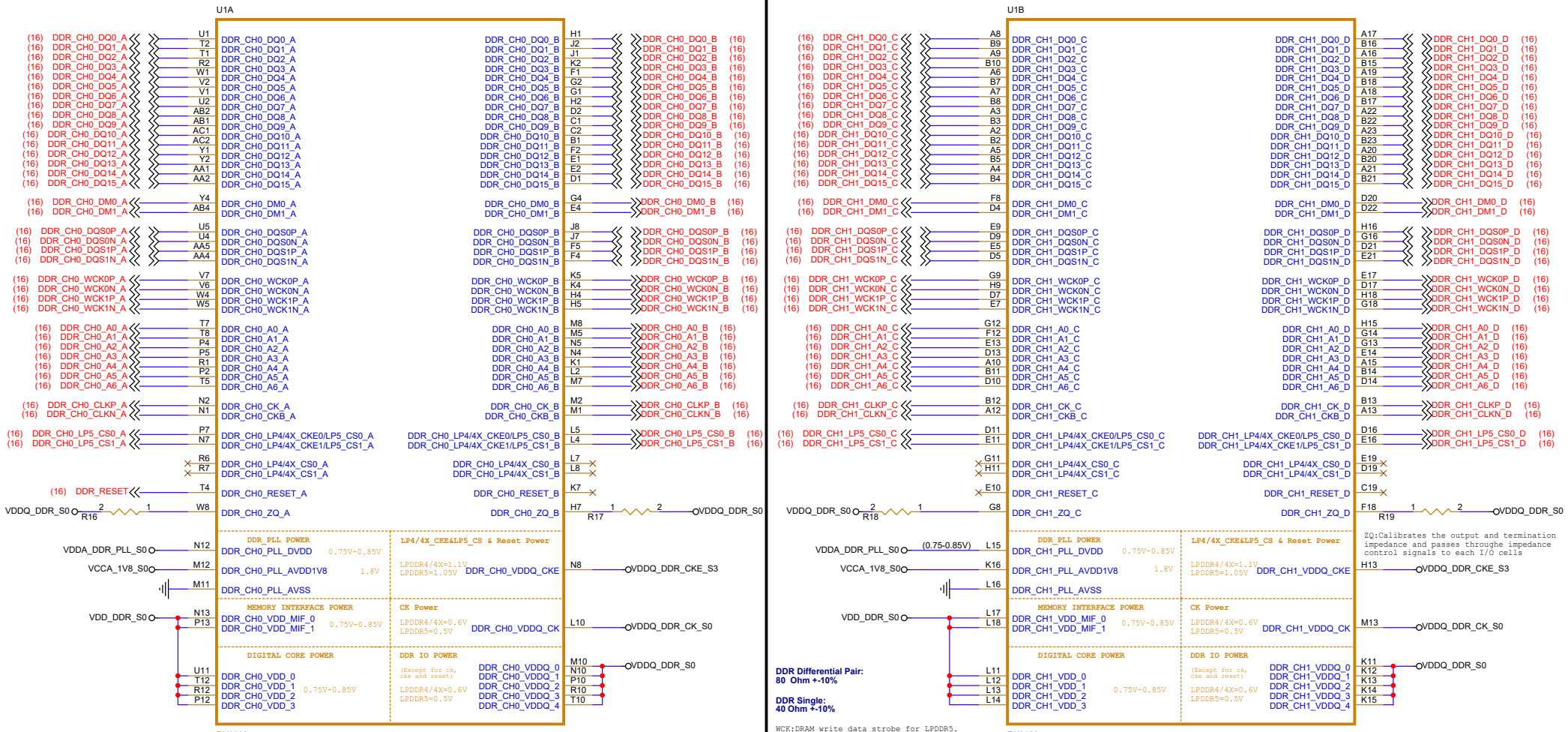


Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

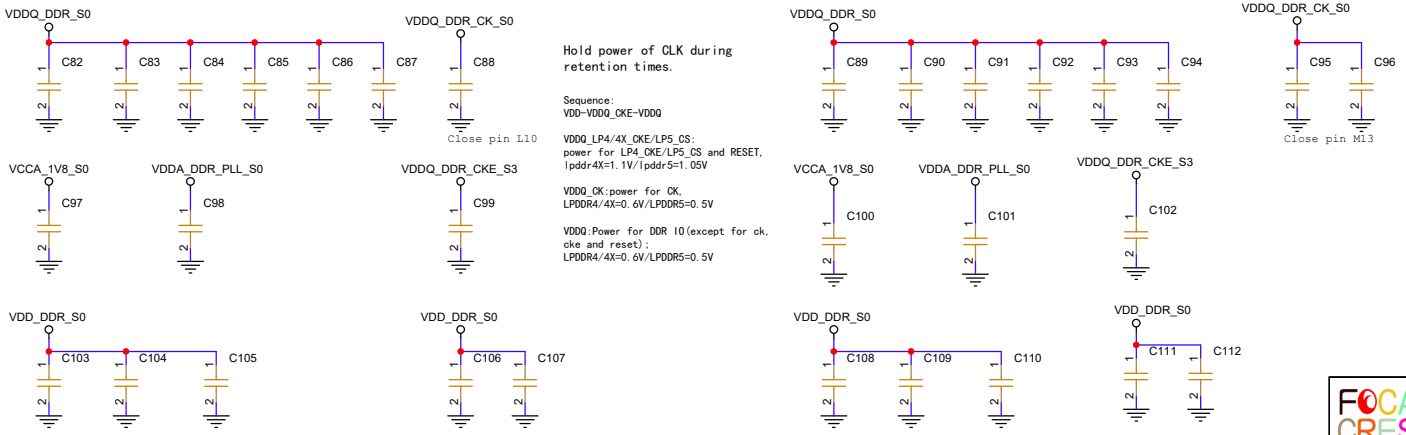
RK3588_F(PMUIO2)



Design Name	CORE3588E_V2.1.0		
Size A3	Page Name 05.RK3588_OSC/PLL/PMUIO	Rev V2.1.0	
Date:		Sheet 5 of 20	

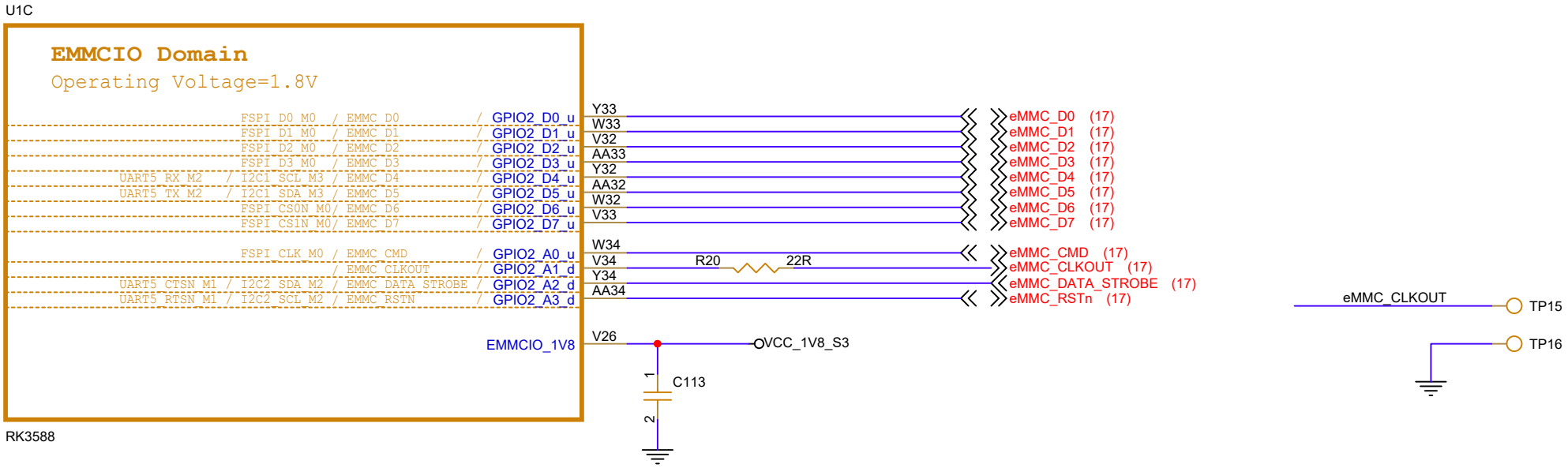


DDR FILTER

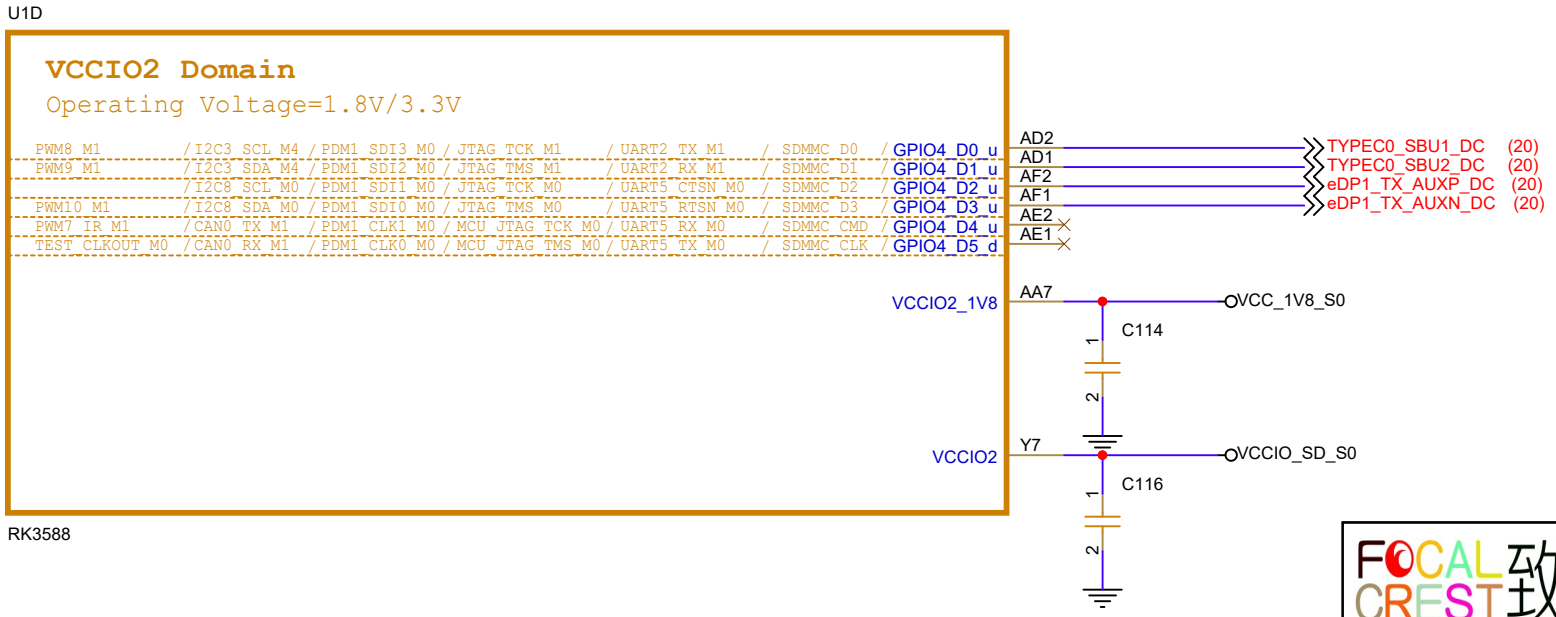


Design Name	CORE3588E_V2.1.0	
Size: Custom	Page Name: 06.RK3588 DDR Controler	Rev: V2.1.0
Date:	Sheet 6 of 20	

RK3588_C(EMMCIO Domain)



RK3588_D(VCCIO2 Domain)



Design Name: CORE3588E_V2.1.0		
Size: A4	Page Name: 07.RK3588_Flash/SD Controller	Rev: V2.1.0
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RK3588_M(TYPEC/DP)

U1M

USB3.0 OTG/DP1.4 Alt of TYPEC0

USB:U3/Gen1----Controller0
DP:RBR/HBR/HBR2/HBR3

TYPEC0_SBU1/DP0_AUXP
TYPEC0_SBU2/DP0_AUXN
TYPEC0_SSRX1P/DP0_TX0P
TYPEC0_SSRX1N/DP0_TX0N
TYPEC0_SSTX1P/DP0_TX1P
TYPEC0_SSTX1N/DP0_TX1N
TYPEC0_SSRX2P/DP0_TX2P
TYPEC0_SSRX2N/DP0_TX2N
TYPEC0_SSTX2P/DP0_TX3P
TYPEC0_SSTX2N/DP0_TX3N
TYPEC0_DP0_REXT
TYPEC0_DP0_VDD_0V85
TYPEC0_DP0_VDDA_0V85
TYPEC0_DP0_VDDH_1V8

AL15 AM15 AN13 AP13 AP14 AN14 AN15 AP15 AP16 AN16 AH16 AJ14 AH14 AG14

TYPEC0_TX1P C403 100nF/10V
TYPEC0_TX1N C404 100nF/10V
TYPEC0_TX2P C405 100nF/10V
TYPEC0_TX2N C406 100nF/10V

R29 C117 C118 C119 C120

VDDA_0V85_S0 VCCA_1V8_S0

Do not delete!!!

Note:
If TYPEC0 is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC&DP MUX Differential Pair:
DATE:95 Ohm +-10%
For Typec

USB30 Differential Pair:
DATE:90 Ohm +-10%
For USB30

DP Differential Pair:
DATE:100 Ohm +-10%
For DP

USB3.0 OTG/DP1.4 Alt of TYPEC1

USB:U3/Gen1----Controller1
DP:RBR/HBR/HBR2/HBR3

TYPEC1_SBU1/DP1_AUXP
TYPEC1_SBU2/DP1_AUXN
TYPEC1_SSRX1P/DP1_TX0P
TYPEC1_SSRX1N/DP1_TX0N
TYPEC1_SSTX1P/DP1_TX1P
TYPEC1_SSTX1N/DP1_TX1N
TYPEC1_SSRX2P/DP1_TX2P
TYPEC1_SSRX2N/DP1_TX2N
TYPEC1_SSTX2P/DP1_TX3P
TYPEC1_SSTX2N/DP1_TX3N
TYPEC1_DP1_REXT
TYPEC1_DP1_VDD_0V85
TYPEC1_DP1_VDDA_0V85
TYPEC1_DP1_VDDH_1V8

AL10 AM10 AN8 AP8 AP9 AN9 AN10 AP10 AP11 AN11 AG16 AH13 AJ13 AG13

TYPEC1_TX1P C121 100nF/10V
TYPEC1_TX1N C123 100nF/10V

R33 C126 C127 C128 C129

VDDA_0V85_S0 VCCA_1V8_S0

Note:
If need full function of Typec1
(With DP funtion)
please Refer to the circuit of Typec0

If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

RK3588

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*TYPEC_SSTX1P/1N&TYPEC_SSRX1P/1N or TYPEC_SSTX2P/2N&TYPEC_SSRX2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1 DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3 DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)

U1L

USB2.0 of TYPEC0 (OTG/HOST/DEVICE)

HS/FS/LS

Download Port

TYPEC0_USB20_OTG_DP
TYPEC0_USB20_OTG_DM
TYPEC0_USB20_OTG_ID
TYPEC0_USB20_VBUSDET
TYPEC0_USB20_OTG0_REXT

AL12 AM12 AL14 AM14 AP12

=1.8V TP1
<=3.3V TYPEC0_USB20_VBUSDET R27 VCCA_3V3_S0
OTG0_REXT R28

TYPEC0_OTG_DP (20)
TYPEC0_OTG_DM (20)

Device/Host/USB Recovery mode.

USB20 Differential Pair:
DATE:90 Ohm +-10%

USB2.0 of TYPEC1 (OTG/HOST/DEVICE)

HS/FS/LS

TYPEC1_USB20_OTG_DP
TYPEC1_USB20_OTG_DM
TYPEC1_USB20_OTG_ID
TYPEC1_USB20_VBUSDET
TYPEC1_USB20_OTG1_REXT

AK9 AL9 AK8 AL8 AP7

TYPEC1_OTG_DP (20)
TYPEC1_OTG_DM (20)
R333
TYPEC1_USB20_VBUSDET R405 VCCA_3V3_S0
OTG1_REXT R30

USB2.0 HOST0

HS/FS/LS

USB20_HOST0_DP
USB20_HOST0_DM
USB20_HOST0_REXT

AK6 AL6 AG9

USB20_HOST0_DP (20)
USB20_HOST0_DM (20)
HOST0_REXT R31

USB2.0 HOST1

HS/FS/LS

USB20_HOST1_DP
USB20_HOST1_DM
USB20_HOST1_REXT

AL7 AM7 AH9

HOST1_REXT R32

USB2.0 POWER

USB20_DVDD_0V75
USB20_AVDD_1V8
USB20_AVDD_3V3

AH10 AG11 AJ10

C122 C124 C125

VDDA_0V75_S0 VCCA_1V8_S0 VCCA_3V3_S0

RK3588

TYPEC1_USB20_VBUSDET (20)

Note:
TYPEC0_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:
If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating
Power:Leave floating

USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating
Power:Leave floating

Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

FOCAL CREST 致趣

Design Name: CORE3588E_V2.1.0
Size: Custom | Page Name: 08.RK3588_USB30/USB20_Ctrl | Rev: V2.1.0
Date: | Sheet 8 of 20

RK3588_G(VCCIO1 Domain)

U1G

VCCIO1 Domain

Operating Voltage=1.8V

SPI4_MISO_M0 / UART3_RX_M0 /		/ I2C3_SDA_M0 /		/	/ GPIO1_C0_z	G29
SPI4_MOSI_M0 / UART3_TX_M0 /		/ I2C3_SCL_M0 /		/	/ GPIO1_C1_z	G27
SPI4_CLK_M0 / UART3_RTSN /	PWM3_IR_M2 /	I2C6_SDA_M1 /		/ I2S0_MCLK	/ GPIO1_C2_d	F30
SPI4_CS0_M0 / UART3_CTSN /	PWM7_IR_M2 /	I2C6_SCL_M1 /		/ I2S0_SCLK	/ GPIO1_C3_d	E31
SPI4_CS1_M0 /	PWM11_IR_M2 /	I2C2_SDA_M3 /	PDM0_CLK1_M0 /		/ GPIO1_C4_d	E30
/ UART4_RTSN /		I2C2_SCL_M3 /		/ I2S0_LRCK	/ GPIO1_C5_d	D30
/	PWM15_IR_M2 /	I2C4_SDA_M4 /	PDM0_CLK0_M0 /		/ GPIO1_C6_d	D29
/ UART4_CTSN /		I2C4_SCL_M4 /		/ I2S0_SDO0	/ GPIO1_C7_d	E29
						F26
SPI1_MISO_M2 / UART6_TX_M2 /		/ I2C7_SCL_M0 /		/ I2S0_SDO1	/ GPIO1_D0_d	F27
SPI1_MOSI_M2 / UART6_RX_M2 /		/ I2C7_SDA_M0 /	PDM0_SDI1_M0 /	I2S0_SDO2/I2S0_SDI3	/ GPIO1_D1_d	F28
SPI1_CLK_M2 / UART4_TX_M0	PWM0_M1	I2C1_SCL_M4	PDM0_SDI2_M0 /	I2S0_SDO3/I2S0_SDI2	/ GPIO1_D2_d	E28
SPI1_CS0_M2 / UART4_RX_M0 /	PWM1_M1	I2C1_SDA_M4 /	PDM0_SDI3_M0 /	I2S0_SDI1	/ GPIO1_D3_d	D28
/		/		/ I2S0_SDI0	/ GPIO1_D4_d	G26
SPI1_CS1_M2 /		/	PDM0_SDI0_M0 /		/ GPIO1_D5_d	

VCCIO1_1V8

G20 — VCC_1V8_S0

C136

I2C3_SDA_M0 (20)

I2C3_SCL_M0 (20)

GPIO09_I2S0_MCLK (20)

I2S0_SCLK (20)

I2S0_LRCK (20)

I2S0_SDO (20)

SPI1_MISO_M2 (20)

SPI1_MOSI_M2 (20)

SPI1_CLK_M2 (20)

SPI1_CS0_M2 (20)

I2S0_SDI (20)

SPI1_CS1_M2 (20)

VCC_1V8_S0

R360 2.2K

R361 2.2K

I2C3_SDA_M0

I2C3_SCL_M0

RK3588

RK3588_U(SARADC/OTP)

U1U

SARADC

12-bit 1MS/s

SARADC_IN0_BOOT Recovery/	AM16	BOOT_SARADC_IN0	
SARADC_IN1	AL16	SARADC_VIN1_KEY/RECOVERY	C130 1 2
SARADC_IN2	AK16		C131 1 2
SARADC_IN3	AN17	SARADC_VIN3_HP_HOOK	C132 1 2
SARADC_IN4	AM17		
SARADC_IN5	AK15	SARADC_VIN5_HW_ID	C133 1 2
SARADC_IN6	AL17	SARADC_VIN6_HW_ID	C504 1 2
SARADC_IN7	AK17		

R34 1 2 VCCA_1V8_S0

SARADC_AVDD_1V8 — AH18 — VCCA_1V8_S0 — C134

OTP

NC — AD4 — Must floating

OTP_VDDOTP_0V75 — AD3 — VDD_0V75_S0 — C135

TSADC

TSADC_TEST_OUT_TS — AF18

SARADC_VIN1_KEY/RECOVERY (20)

RK3588

BOOT MODE CONFIG

TP2

VCCA_1V8_S0

R35 100K

BOOT_SARADC_IN0

R36 NC/100K

TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

VCCA_1V8_S0

R43 100K

SARADC_VIN5_HW_ID

R45 20K

VCCA_1V8_S0

R403 100K

SARADC_VIN6_HW_ID

R404 20K

TABLE 2

	ADC5			ADC6			
Item	Rup	Rdown	ADC	Rup	Rdown	ADC	VERSION
LEVEL1	DNP	100K	0	DNP	100K	0	V2.0.0
LEVEL2	100K	20K	682	100K	20K	682	V2.1.0
LEVEL3	100K	51K	1365	100K	51K	1365	RESERVE
LEVEL4	100K	100K	2047	100K	100K	2047	RESERVE
LEVEL5	100K	200K	2730	100K	200K	2730	RESERVE
LEVEL6	100K	499K	3412	100K	499K	3412	RESERVE
LEVEL7	100K	DNP	4095	100K	DNP	4095	RESERVE

RK3588_H(VCCIO3 Domain)

U1H

VCCIO3 Domain

Operating Voltage=1.8V

All this bank is only 1.8V

	/ UART6_RX_M0	/ FSPI_D0_M1	/ SDIO_D0_M0	/ GMAC0_RXD2	/ GPIO2_A6_u	AC32
	/ UART6_TX_M0	/ FSPI_D1_M1	/ SDIO_D1_M0	/ GMAC0_RXD3	/ GPIO2_A7_u	AC31
I2C8_SCL_M1	/ UART6_RTSN_M0	/ FSPI_D2_M1	/ SDIO_D2_M0	/ GMAC0_RXCLK	/ GPIO2_B0_u	AE32
I2C8_SDA_M1	/ UART6_CTSN_M0	/ FSPI_D3_M1	/ SDIO_D3_M0	/ GMAC0_TXD2	/ GPIO2_B1_u	AC33
I2C3_SCL_M3	/	/	/ SDIO_CMD_M0	/ GMAC0_TXD3	/ GPIO2_B2_u	AC34
I2C3_SDA_M3	/	/ FSPI_CLK_M1	/ SDIO_CLK_M0	/ GMAC0_TXCLK	/ GPIO2_B3_d	AE33
I2C4_SDA_M1	/ UART7_RX_M0	/ FSPI_CSON_M1	/ HDMI_TX1_SDA_M0	/ GMAC0_PTP_REFCLK	/ GPIO2_B4_u	AB31
I2C4_SCL_M1	/ UART7_TX_M0	/ FSPI_CSIN_M1	/ HDMI_TX1_SCL_M0	/ GMAC0_PPSTRIG	/ GPIO2_B5_u	AB30
I2C5_SCL_M1	/ UART7_RX_M0	/	/ I2S1_MCLK_M0	/ GMAC0_TXD0	/ GPIO2_B6_d	AD33
I2C5_SDA_M1	/ UART7_TX_M0	/	/ I2S1_SCLK_M0	/ GMAC0_TXD1	/ GPIO2_B7_d	AD34
						AE34
I2C2_SDA_M1	/ UART1_RTSN_M0	/ SPI1_CLK_M0	/ I2S2_LRCK_M0	/ GMAC0_TXEN	/ GPIO2_C0_d	AD32
I2C2_SCL_M1	/ UART1_CTSN_M0	/ SPI1_MISO_M0	/	/ GMAC0_RXD0	/ GPIO2_C1_d	AD31
I2C6_SDA_M2	/ UART9_TX_M0	/ SPI1_MOSI_M0	/	/ GMAC0_RXD1	/ GPIO2_C2_d	AD30
I2C6_SCL_M2	/	/ SPI1_CS0_M0	/ I2S2_SDX_M0	/ ETH0_REFCLKO_25M	/ GPIO2_C3_d	AC30
TEST_CLKOUT_M1	/ UART9_RX_M0	/ SPI1_CS1_M0	/ HDMI_TX1_CEC_M0	/ GMAC0_PPSCLK	/ GPIO2_C4_d	AE30
	/	/	/	/ CLK32K_OUT1	/ GPIO2_C5_d	
						AE31
	/ UART7_RTSN_M0	/ SPI3_CS0_M0	/ PWM2_M2	/ GMAC0_RXDV_CRS	/ GPIO4_C2_d	AF34
I2C7_SCL_M1	/ PWM4_M1	/ SPI3_CS1_M0	/ I2S2_SDO_M0	/ GMAC0_MCLRINOUT	/ GPIO4_C3_d	AB34
I2C7_SDA_M1	/ UART9_RTSN_M0	/ SPI3_MISO_M0	/ PWM5_M2	/ GMAC0_MDC	/ GPIO4_C4_d	AB33
I2C0_SCL_M1	/ UART9_CTSN_M0	/ SPI3_MOSI_M0	/ PWM6_M2	/ GMAC0_MDIO	/ GPIO4_C5_d	AF33
I2C0_SDA_M1	/ UART7_CTSN_M0	/ SPI3_CLK_M0	/ PWM7_IR_M3	/ GMAC0_TXER	/ GPIO4_C6_d	

VCCIO3_1V8

Y26 — VCC_1V8_S0

C137

FSPI_SI (17)

FSPI_SO (17)

FSPI_WP (17)

FSPI_HOLD (17)

FSPI_SCLK (17)

FSPI_CS (17)

(GMAC0_TX*)RGMII TX bus length match in 30mils

(GMAC0_RX*)RGMII RX bus length match in 30mils

single-ended impedance 50 Ohm +-10%

RK3588

Design Name	CORE3588E_V2.1.0
Size	A3
Page Name	09.RK3588_SARADC/1.8V Only GPIO
Rev	V2.1.0
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RK3588_Q/R(MIPI_D/C_PHY0/1)

U1Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C — AN26
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B — AP26
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B — AN24
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A — AP24
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A — AN25
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C — AP25
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B — AN27
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A — AP27
MIPI_DPHY0_TX_D3P/NO_USE_AN28 — AN28
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C — AP28

MIPI D/C-PHY CSI_RX Port0

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C — AN32
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B — AP31
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B — AN29
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A — AP29
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A — AN30
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C — AP30
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B — AN33
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A — AP32
MIPI_DPHY0_RX_D3P/NO_USE_AN34 — AN34
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C — AP33

MIPI_CSI4_RX_CLK0P (20) — AN32
MIPI_CSI4_RX_CLK0N (20) — AP31
MIPI_CSI4_RX_D0P (20) — AN29
MIPI_CSI4_RX_D0N (20) — AP29
MIPI_CSI4_RX_D1P (20) — AN30
MIPI_CSI4_RX_D1N (20) — AP30

MIPI DPHY Differential Pair: 100 Ohm +-10%
MIPI CPHY Single: 50 Ohm +-10%

Note:
此D-PHY使用受限!!!
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

Note:
Suggest Using 1/2 lane mode, Using 4Lane is limited, Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG — AF20 — C138 (1, 2)
MIPI_D/C_PHY0_VDD — AG20 — C140, C141 — VDD_0V75_S0
C-PHY 5.7Gbps 0.85V
D-PHY 2.5Gbps & C-PHY 5.7Gbps 0.75V
MIPI_D/C_PHY0_VDD_1V2 — AH20 — C143 — VDDA_1V2_S0
MIPI_D/C_PHY0_VDD_1V8 — AJ20 — C145 — VCC_1V8_S0

RK3588

U1R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C — AN20
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B — AP20
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B — AN18
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A — AP18
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A — AN19
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C — AP19
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B — AN21
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A — AP21
MIPI_DPHY1_TX_D3P/NO_USE_AN22 — AN22
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C — AP22

MIPI D/C-PHY CSI_RX Port1

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C — AK20
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B — AL20
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B — AK18
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A — AL18
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A — AK19
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C — AL19
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B — AK21
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A — AL21
MIPI_DPHY1_RX_D3P/NO_USE_AK22 — AK22
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C — AL22

MIPI_CSI5_RX_CLK0P (20) — AK20
MIPI_CSI5_RX_CLK0N (20) — AL20
MIPI_CSI5_RX_D0P (20) — AK18
MIPI_CSI5_RX_D0N (20) — AL18
MIPI_CSI5_RX_D1P (20) — AK19
MIPI_CSI5_RX_D1N (20) — AL19

Note:
此D-PHY使用受限!!!
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

Note:
Suggest Using 1/2 lane mode, Using 4Lane is limited, Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG — AF19 — C139 (1, 2)
MIPI_D/C_PHY1_VDD — AG19 — C142 — VDD_0V75_S0
MIPI_D/C_PHY1_VDD_1V2 — AH19 — C144 — VDDA_1V2_S0
MIPI_D/C_PHY1_VDD_1V8 — AJ19 — C146 — VCC_1V8_S0

Note:
If not used:
Signal:leave floating
Power: Floating

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RK3588_P(MIPI_DPHY_CSI_RX_PHY)

U1P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P — AJ33
MIPI_CSI0_CLK0N — AJ34
MIPI_CSI0_D0P — AG33
MIPI_CSI0_D0N — AG34
MIPI_CSI0_D1P — AH33
MIPI_CSI0_D1N — AH34
MIPI_CSI0_CLK1P — AM33
MIPI_CSI0_CLK1N — AM34
MIPI_CSI0_D2P — AK33
MIPI_CSI0_D2N — AK34
MIPI_CSI0_D3P — AL33
MIPI_CSI0_D3N — AL34

MIPI_CSI0_RX_CLK0P (20)
MIPI_CSI0_RX_CLK0N (20)
MIPI_CSI0_RX_D0P (20)
MIPI_CSI0_RX_D0N (20)
MIPI_CSI0_RX_D1P (20)
MIPI_CSI0_RX_D1N (20)
MIPI_CSI1_RX_CLK1P (20)
MIPI_CSI1_RX_CLK1N (20)
MIPI_CSI1_RX_D0P (20)
MIPI_CSI1_RX_D0N (20)
MIPI_CSI1_RX_D1P (20)
MIPI_CSI1_RX_D1N (20)

MIPI CSI Differential Pair: 100 Ohm +-10%

MIPI_CSI0_AVCC0V75 — AB25 — C147, C148 — VDD_0V75_S0
MIPI_CSI0_AVCC1V8 — AB26 — C149 — VCC_1V8_S0

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P — AJ31
MIPI_CSI1_CLK0N — AJ32
MIPI_CSI1_D0P — AG31
MIPI_CSI1_D0N — AG32
MIPI_CSI1_D1P — AH31
MIPI_CSI1_D1N — AH32
MIPI_CSI1_CLK1P — AM31
MIPI_CSI1_CLK1N — AM32
MIPI_CSI1_D2P — AK31
MIPI_CSI1_D2N — AK32
MIPI_CSI1_D3P — AL31
MIPI_CSI1_D3N — AL32

MIPI_CSI2_RX_CLKP (20)
MIPI_CSI2_RX_CLKN (20)
MIPI_CSI2_RX_D0P (20)
MIPI_CSI2_RX_D0N (20)
MIPI_CSI2_RX_D1P (20)
MIPI_CSI2_RX_D1N (20)
MIPI_CSI3_RX_CLKP (20)
MIPI_CSI3_RX_CLKN (20)
MIPI_CSI3_RX_D0P (20)
MIPI_CSI3_RX_D0N (20)
MIPI_CSI3_RX_D1P (20)
MIPI_CSI3_RX_D1N (20)

MIPI_CSI1_AVCC0V75 — AA25 — C150 — VDD_0V75_S0
MIPI_CSI1_AVCC1V8 — AA26 — C151 — VCC_1V8_S0

RK3588

Note:
建义优先使用U1000P这个模块的DPHY CSI_RX。
First use the DPHY_CSI_RX controller of U1000P.

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating

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Design Name	CORE3588E_V2.1.0
Size: Custom	Page Name: 10.RK3588_MIPI_Interface
Rev	V2.1.0
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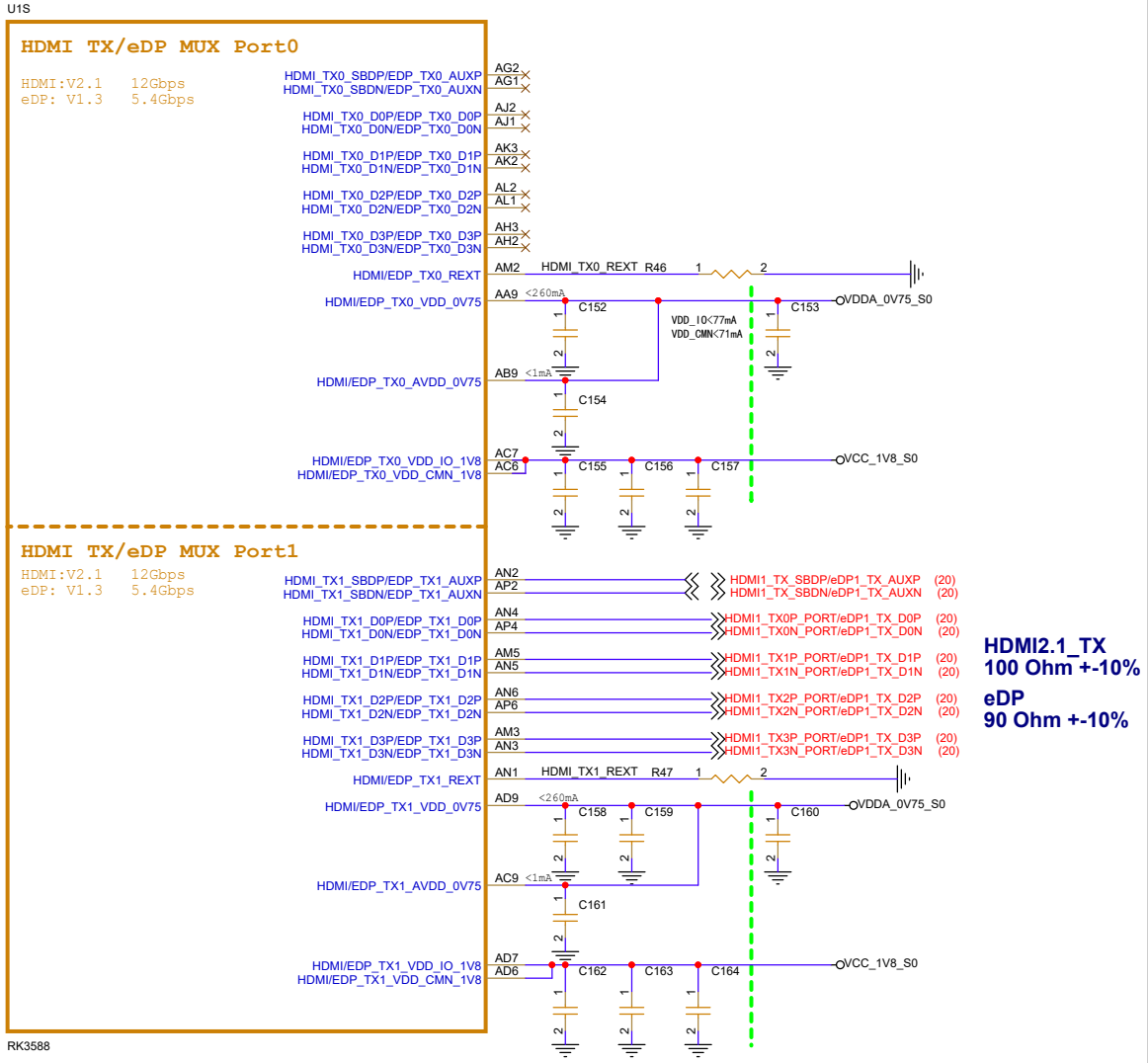
RK3588_S(HDMI2.1 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



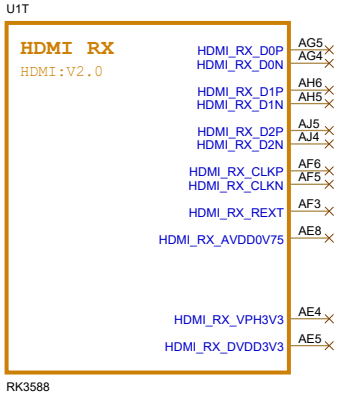
HDMI2.1_TX
100 Ohm +-10%

eDP
90 Ohm +-10%

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

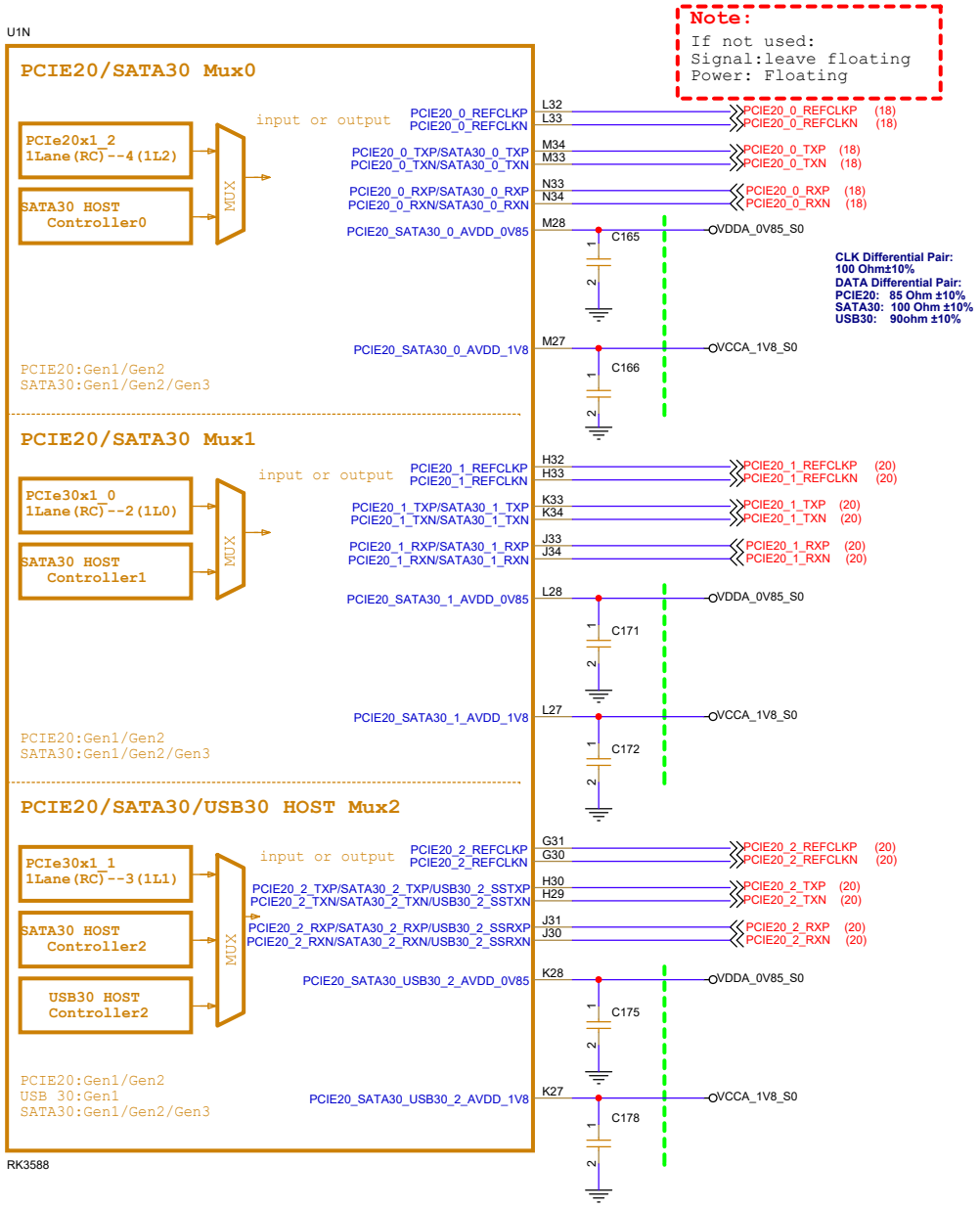
Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

RK3588_T(HDMI20 RX)



Design Name	CORE3588E_V2.1.0	
Size A3	Page Name 11.RK3588_HDMI/eDP Interface	Rev V2.1.0
Date:	Sheet 11 of 20	

RK3588_N(PCIE20)

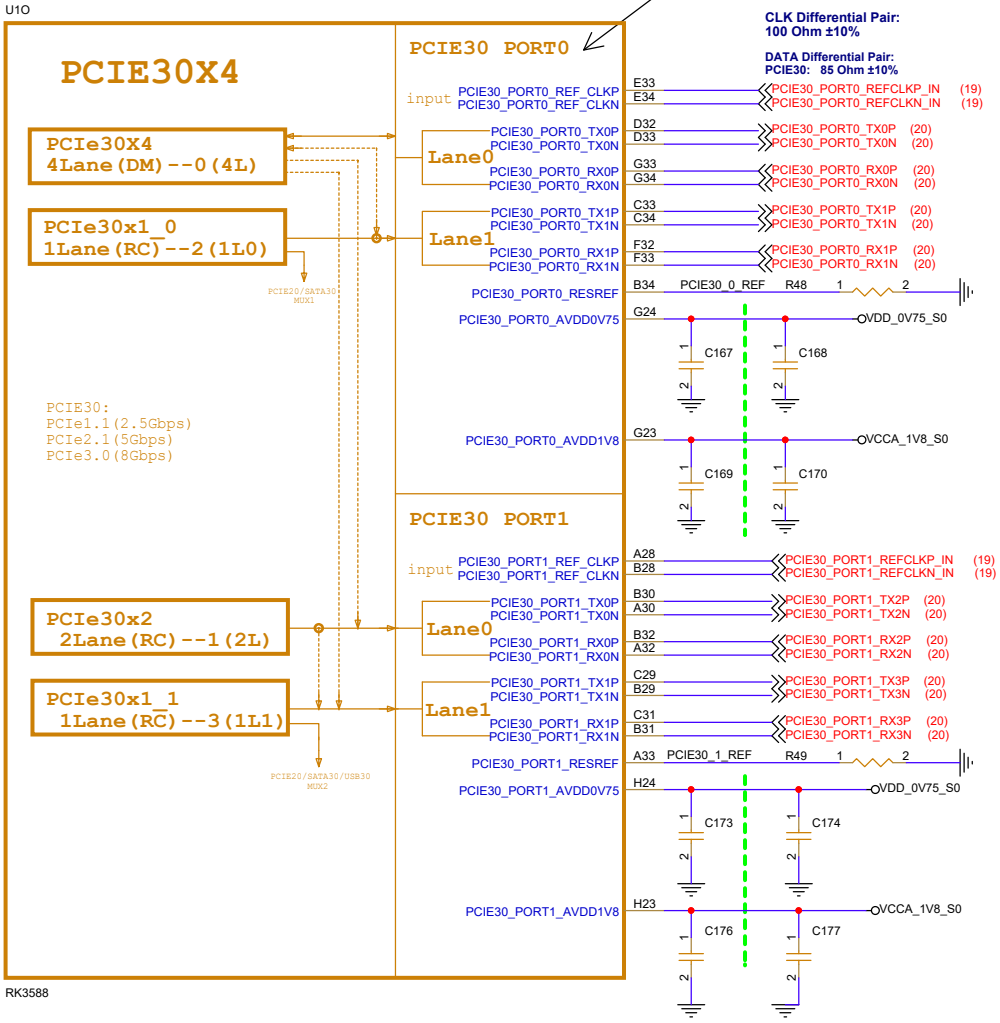


Note:
If not used:
Signal:leave floating
Power: Floating

Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

RK3588_O(PCIE30)

Note:
Only PCIE3.0 Controller 0 support RC and EP,Other controller only support RC Mode.



Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

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Design Name: CORE3588E_V2.1.0		
Size: A3	Page Name: 12.RK3588_PCIE30/PCIE20/SATA30	Rev: V2.1.0
Date:	Sheet: 12 of 20	

RK3588_J(VCCIO5 Domain)

U1J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1	I2C6_SDA_M4	FSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u
AUDDSM_LN	SPI4_MOSI_M1	PWM11_IR_M0	I2C6_SCL_M4	FSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u
AUDDSM_LP	SPI4_CLK_M1	UART9_TX_M1		FSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u
AUDDSM_RN	SPI4_CS0_M1	UART9_RX_M1		FSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u
AUDDSM_RP	SPI4_CS1_M1	UART9_RTSN_M1			I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d
	MIPI_CAMERA0_CLK_M1	UART9_CTSN_M1	I2C4_SDA_M0	FSPI_CLK_M2		SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d
	MIPI_CAMERA1_CLK_M1		I2C4_SCL_M0				ETH1_REFCLKO_25M	GPIO3_A6_d
PWM8_M0	MIPI_CAMERA2_CLK_M1						GMAC1_RXD0	GPIO3_A7_u
PWM9_M0	MIPI_CAMERA3_CLK_M1						GMAC1_RXD1	GPIO3_B0_u
PWM2_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2					GMAC1_RXDV_CRS	GPIO3_B1_d
PWM3_IR_M1		UART2_RX_M2			I2S2_SDI_M1		GMAC1_TXER	GPIO3_B2_d
		UART2_RTSN			I2S2_SDO_M1		GMAC1_TXD0	GPIO3_B3_u
		UART2_CTSN			I2S2_MCLK_M1		GMAC1_TXD1	GPIO3_B4_u
PWM12_M0	CAN1_RX_M0	UART3_TX_M1			I2S2_SCLK_M1		GMAC1_TXEN	GPIO3_B5_u
PWM13_M0	CAN1_TX_M0	UART3_RX_M1			I2S2_LRCK_M1		GMAC1_MCLKINOUT	GPIO3_B6_d
			I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1		GMAC1_PTP_REF_CLK	GPIO3_B7_d
		UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1			GMAC1_PPSTRIG	GPIO3_C0_d
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1		SPI1_CLK_M1			GMAC1_PPSCLK	GPIO3_C1_d
PWM14_M0		UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1		MIPI_TE0	GMAC1_MDC	GPIO3_C2_d
PWM15_IR_M0		UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1		MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d
CAN2_RX_M0	PCIE30X4_CLKREQN_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2		CIF_D8	GPIO3_C4_u
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1		CIF_D9	GPIO3_C5_u
	PCIE30X4_PERSTN_M2			SPI3_MISO_M3	HDMI_TX1_SCL_M1		CIF_D10	GPIO3_C6_u
	PCIE20X1_2_CLKREQN_M0		I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2		CIF_D11	GPIO3_C7_u
PWM8_M2	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2		CIF_D12	GPIO3_D0_u
PWM9_M2	PCIE20X1_2_PERSTN_M0	UART4_TX_M1		SPI0_MISO_M3	HDMI_RX_CEC_M1		CIF_D13	GPIO3_D1_d
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1		CIF_D14	GPIO3_D2_d
PWM10_M2	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1		CIF_D15	GPIO3_D3_d
	PCIE30X2_PERSTN_M2	UART9_RX_M2		SPI0_CS0_M3	HDMI_RX_HPDOUT_M1	HDMI_TX0_HPD_M1	MCU_JTAG_TCK_M1	GPIO3_D4_d
PWM11_IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2		SPI0_CS1_M3	DP1_HPDIN_M0		MCU_JTAG_TMS_M1	GPIO3_D5_d

AA29	GPIO3_A0_u	GPIO07_PWM10 (20)
AA30	GPIO3_A1_u	I2S3_SCLK (20)
AD27	GPIO3_A2_u	I2S3_LRCK (20)
AE27	GPIO3_A3_u	I2S3_SDO (20)
AD28	GPIO3_A4_d	I2S3_SDI (20)
AH30	GPIO3_A5_d	MIPI_CAM0_MCLK_M1 (20)
AH27	GPIO3_A6_d	MIPI_CAM1_MCLK_M1 (20)
AG29	GPIO3_A7_u	GPIO00 (20)
AG28	GPIO3_B0_u	GPIO13_PWM9 (20)
AH29	GPIO3_B1_d	GPIO14_PWM2 (20)
AE28	GPIO3_B2_d	I2S2_SDI (20)
AC28	GPIO3_B3_u	I2S2_SDO (20)
AC29	GPIO3_B4_u	GPIO08_FAN_TACH (20)
AD29	GPIO3_B5_u	I2S2_SCLK (20)
AE29	GPIO3_B6_d	I2S2_LRCK (20)
AA28	GPIO3_B7_d	EDP1_HPD (20)
Y29	GPIO3_C0_d	UART7_TX_M1 (20)
Y27	GPIO3_C1_d	UART7_RX_M1 (20)
Y31	GPIO3_C2_d	UART7_RTSN_M1 (20)
Y30	GPIO3_C3_d	UART7_CTSN_M1 (20)
AH26	GPIO3_C4_u	HDMI_TX0_CEC_M0 (20)
AH25	GPIO3_C5_u	HDMI_TX0_SDA_M0 (20)
AG26	GPIO3_C6_u	HDMI_TX0_SCL_M0 (20)
AJ24	GPIO3_C7_u	PCIE20_2_CLKREQn (20)
AH24	GPIO3_D0_u	TP14
AG23	GPIO3_D1_d	SPI0_MISO_M3 (20)
AG25	GPIO3_D2_d	SPI0_MOSI_M3 (20)
AG24	GPIO3_D3_d	SPI0_CLK_M3 (20)
AA27	GPIO3_D4_d	GPIO11 (20)
AB28	GPIO3_D5_d	SPI0_CS1_M3 (20)

R52 1 2 0R

VCCIO5_1V8: W25 — C181 — VCC_1V8_S0

VCCIO5: W26 — C182 — VCC_1V8_S0

RK3588

RK3588_K(VCCIO6 Domain)

U1K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	SPI0_MISO_M1	UART9_RTSN_M1		I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d
	SPI0_MOSI_M1	UART9_CTSN_M1		I2S1_SCLK_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d
	SPI0_CLK_M1			I2S1_LRCK_M0	PCIE30X1_1_PERSTN_M1	BT1120_D2	CIF_D2	GPIO4_A2_d
		UART0_TX_M2			PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d
	SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2		PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d
	SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2	I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d
	SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2	I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d
	SPI2_CS0_M1		I2C5_SDA_M2	I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d
	SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3	I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3	I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN		MIPI_CAMERA0_CLK_M0	GPIO4_B1_u
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3	I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u
CAN1_TX_M1	PWM15_IR_M1		UART8_CTSN_M0	I2C7_SDA_M3	I2S1_SDO2_M0	PCIE20X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u
SPDIF0_TX_M1	PWM11_IR_M1	DP0_HPDIN_M0	UART9_TX_M1		I2S1_SDO3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u
SATA1_ACT_LED_M0	PWM12_M1	SPI3_MISO_M1	UART9_RX_M1		HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11		GPIO4_B5_d
SATA0_ACT_LED_M0	PWM13_M1	SPI3_MOSI_M1		I2C5_SCL_M1	HDMI_RX_HPDOUT_M0	PCIE30X4_PERSTN_M1	BT1120_D12		GPIO4_B6_d
		SPI3_CLK_M1		I2C5_SDA_M1	HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13		GPIO4_B7_u
		SPI3_CS0_M1		I2C8_SCL_M3	HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14		GPIO4_C0_u
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1		I2C8_SDA_M3	HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15		GPIO4_C1_d

AK30	GPIO4_A0_d	GPIO15 (20)
AL30	GPIO4_A1_d	I2S1_SCLK_M0 (20)
AM29	GPIO4_A2_d	I2S1_LRCK_M0 (20)
AL29	GPIO4_A3_d	LAN_DISABLE_N (18)
AL28	GPIO4_A4_d	LAN_PWR_GOOD (18)
AK27	GPIO4_A5_d	I2S1_SDI_M0 (20)
AL27	GPIO4_A6_d	I2C5_SCL_M2 (20)
AM27	GPIO4_A7_d	I2C5_SDA_M2 (20)
AK26	GPIO4_B0_d	GPIO_CLK (19)
AL24	GPIO4_B1_u	I2S1_SDO_M0 (20)
AK25	GPIO4_B2_u	CAN1_RX_M1 (20)
AM25	GPIO4_B3_u	CAN1_TX_M1 (20)
AL26	GPIO4_B4_u	PCIE30X4_CLKREQn_M1_L (20)
AJ26	GPIO4_B5_d	PCIE30X4_WAKEn_M1_L/GPIO4_B5 (20)
AJ27	GPIO4_B6_d	PCIE30X4_PERSTn_M1_L (20)
AJ28	GPIO4_B7_u	PCIE20_0_CLKREQn (18)
AJ25	GPIO4_C0_u	PCIE20_0_WAKEn (18)
AK24	GPIO4_C1_d	PCIE20_0_PERSTn (18)

VCC_3V3_S0 — R50 2.2K — R51 2.2K — I2C5_SCL_M2 / I2C5_SDA_M2

VCCIO6_1V8: AC25 — C179 — VCC_1V8_S0

VCCIO6: AC26 — C180 — VCC_3V3_S0

RK3588

RK3588_I(VCCIO4 Domain)

U1I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

	SPI4_MISO_M2	PCIE30X1_1_CLKREQN_M2	DP0_HPDIN_M2	I2C2_SDA_M4	UART6_RX_M1	GPIO1_A0_d
SATA1_ACT_LED_M1	SPI4_MOSI_M2	PCIE30X1_1_WAKEN_M2	DP1_HPDIN_M2	I2C2_SCL_M4	UART6_TX_M1	GPIO1_A1_d
PWM0_M2	SPI4_CLK_M2		VOP_POST_EMPTY	I2C4_SDA_M3	UART6_RTSN_M1	GPIO1_A2_d
PWM1_M2	SPI4_CS0_M2		HDMI_TX1_SDA_M2	I2C4_SCL_M3	UART6_CTSN_M1	GPIO1_A3_d
	SPI2_MISO_M0		HDMI_TX1_SCL_M2			GPIO1_A4_d
	SPI2_MOSI_M0		HDMI_TX0_HPD_M0			GPIO1_A5_d
	SPI2_CLK_M0		HDMI_TX1_HPD_M0			GPIO1_A6_d
PWM3_IR_M3	SPI2_CS0_M0	PCIE30X1_1_PERSTN_M2		PDM1_SDI0_M1		GPIO1_A7_u
	SPI2_CS1_M0	PCIE30X4_CLKREQN_M3		PDM1_SDI1_M1		GPIO1_B0_u
	SPI0_MISO_M2	PCIE30X4_WAKEN_M3		PDM1_SDI2_M1		GPIO1_B1_d
	SPI0_MOSI_M2	PCIE30X4_PERSTN_M3		PDM1_SDI3_M1	UART4_RX_M2	GPIO1_B2_d
SATA0_ACT_LED_M1	SPI0_CLK_M2	PCIE30X1_0_WAKEN_M2		PDM1_CLK1_M1	UART4_TX_M2	GPIO1_B3_d
	SPI0_CS0_M2	PCIE30X1_0_PERSTN_M2		PDM1_CLK0_M1	UART7_RX_M2	GPIO1_B4_u
	SPI0_CS1_M2	PCIE30X1_0_CLKREQN_M2			UART7_TX_M2	GPIO1_B5_u
HDMI_RX_HPDOUT_M2	SPDIF0_TX_M0	PCIE30X2_WAKEN_M3	MIPI_CAMERA1_CLK_M0	I2C5_SCL_M3	UART1_TX_M1	GPIO1_B6_u
SATA2_ACT_LED_M1 HDMI_RX_CEC_M2	PWM13_M2	SPDIF1_TX_M0	PCIE30X2_PERSTN_M3	MIPI_CAMERA2_CLK_M0	I2C5_SDA_M3	UART1_RX_M1	GPIO1_B7_u
HDMI_RX_SCL_M2	PWM14_M2		MIPI_CAMERA3_CLK_M0	I2C8_SCL_M2	UART1_RTSN_M1	GPIO1_D6_u
HDMI_RX_SDA_M2	PWM15_IR_M3	PCIE30X2_CLKREQN_M3	MIPI_CAMERA4_CLK_M0	I2C8_SDA_M2	UART1_CTSN_M1	GPIO1_D7_u

A24	GPIO1_A0_d	I2C2_SDA_M4_MIPI (20)
A25	GPIO1_A1_d	I2C2_SCL_M4_MIPI (20)
A26	GPIO1_A2_d	I2C4_SDA_M3 (20)
A27	GPIO1_A3_d	I2C4_SCL_M3 (20)
B25	GPIO1_A4_d	
B26	GPIO1_A5_d	
C24	GPIO1_A6_d	PCIE20_2_RSTn (20)
C25	GPIO1_A7_u	MODULE_ID (20)
C27	GPIO1_B0_u	MIPI_CAM0_PWDN (20)
D25	GPIO1_B1_d	MIPI_CAM1_PWDN (20)
D26	GPIO1_B2_d	PCIE_PWREN_H (19)
D27	GPIO1_B3_d	PCIEx1_0_WAKEn_M2_L/GPIO1_B3 (20)
E24	GPIO1_B4_u	PCIEx1_0_PERSTn_M2_L (20)
E25	GPIO1_B5_u	PCIEx1_0_CLKREQn_M2_L (20)
E26	GPIO1_B6_u	UART1_TX_M1 (20)
E27	GPIO1_B7_u	UART1_RX_M1 (20)
F24	GPIO1_D6_u	UART1_RTSN_M1 (20)
F25	GPIO1_D7_u	UART1_CTSN_M1 (20)

VCCIO4_1V8: H20 — C183 — VCC_1V8_S0

VCCIO4: H21 — C184 — VCC_3V3_S0

RK3588

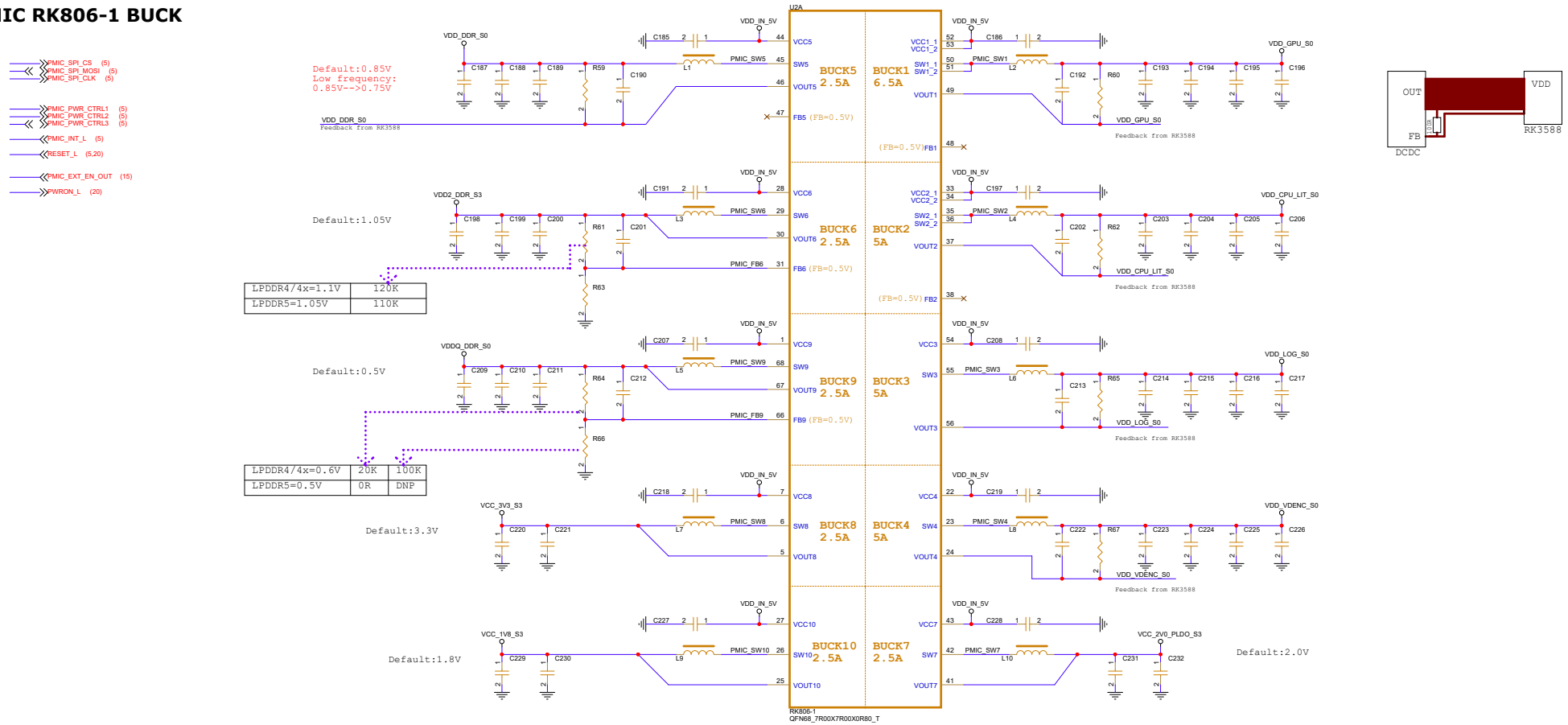
VCC_3V3_S0 — R53 2.2K — R54 2.2K — I2C2_SDA_M4_MIPI / I2C2_SCL_M4_MIPI

VCC_3V3_S0 — R55 2.2K — R56 2.2K — I2C4_SDA_M3 / I2C4_SCL_M3

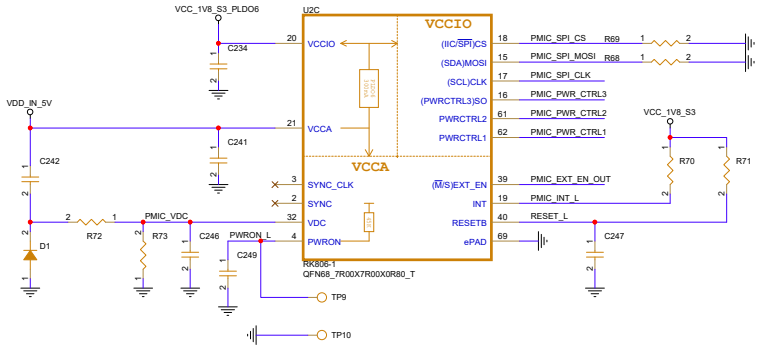
FOCAL CREST 致趣

Design Name	CORE3588E_V2.1.0
Size: Custom	Page Name: 13.RK3588_1.8V/3.3V GPIO
Rev	V2.1.0
Date:	Sheet 13 of 20

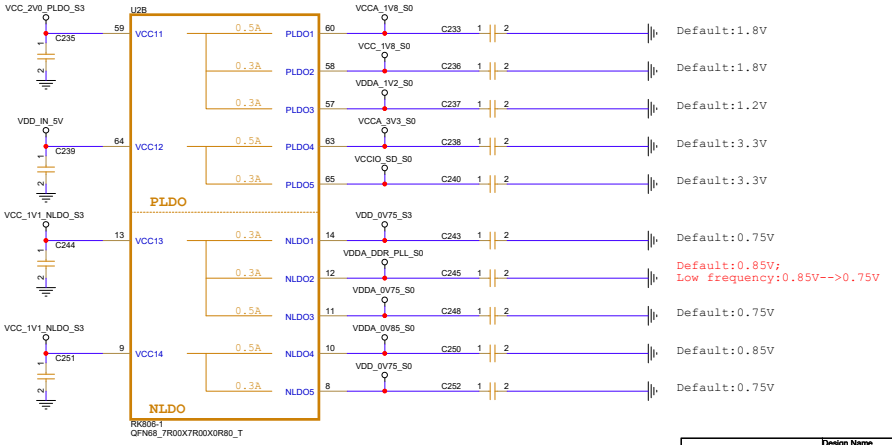
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment



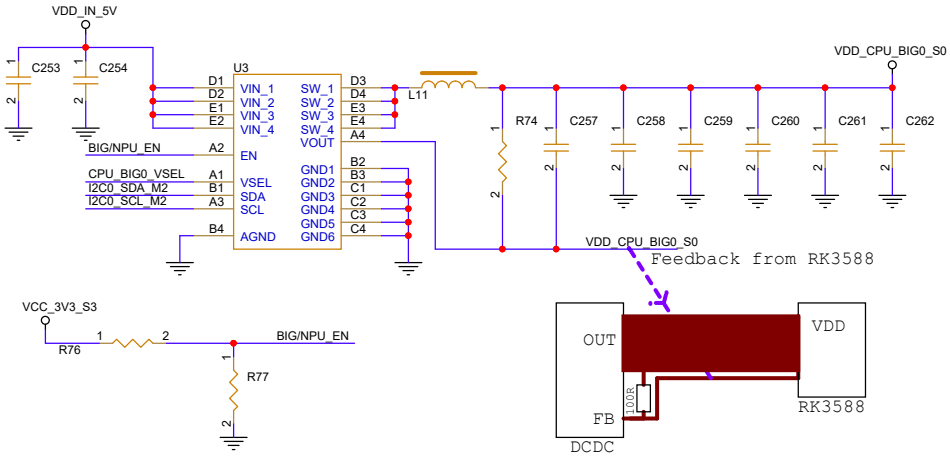
PMIC RK806-1 LDO



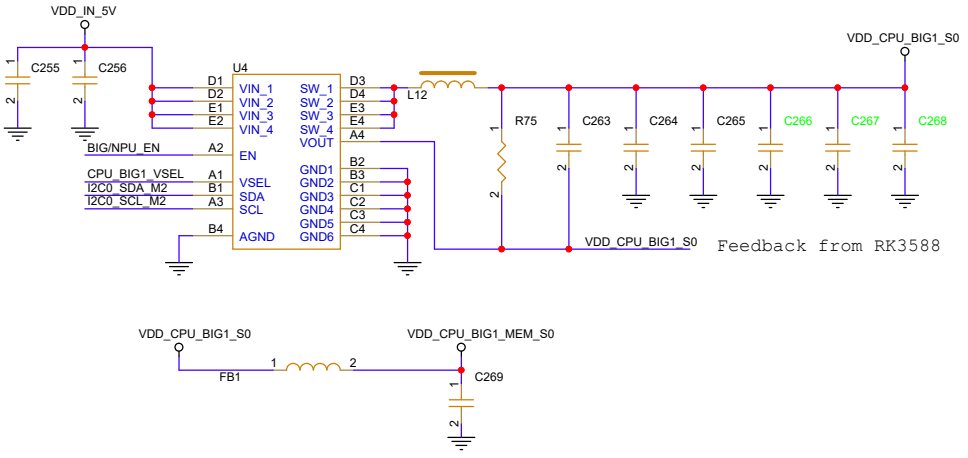
FOCAL CREST 致趣

Design Name	CORE3588E_V2.1.0		
Size A2	Page Name 14.Power-PMIC_RK806-1	Rev V2.1.0	
Date:		Sheet 14 of 20	

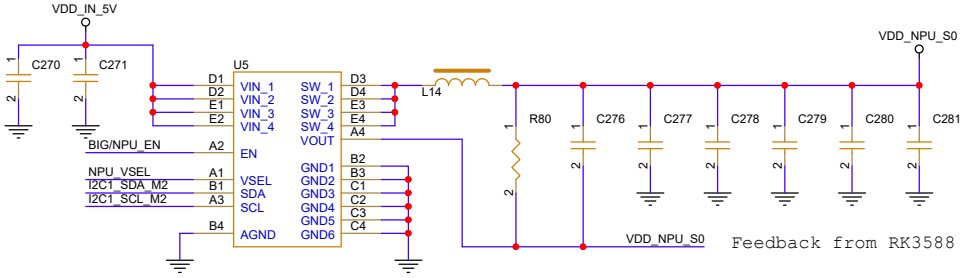
VDD_CPU_BIG0



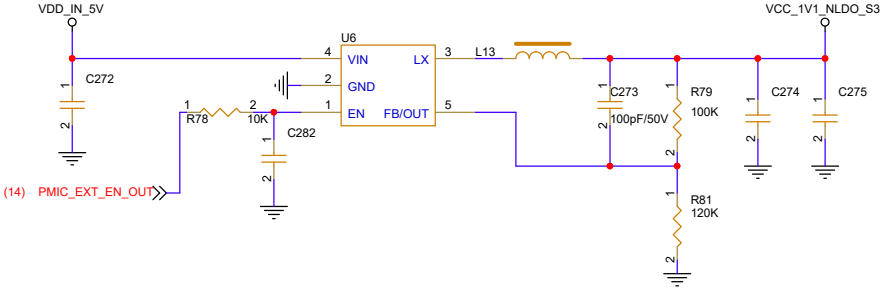
VDD_CPU_BIG1

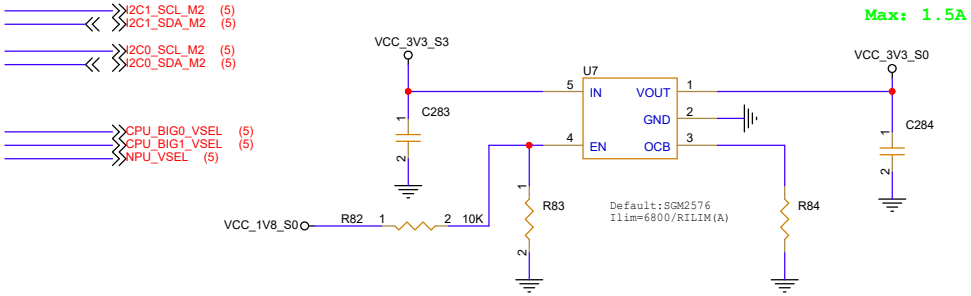


VDD_NPU



VCC_1V1_NLDO_S3

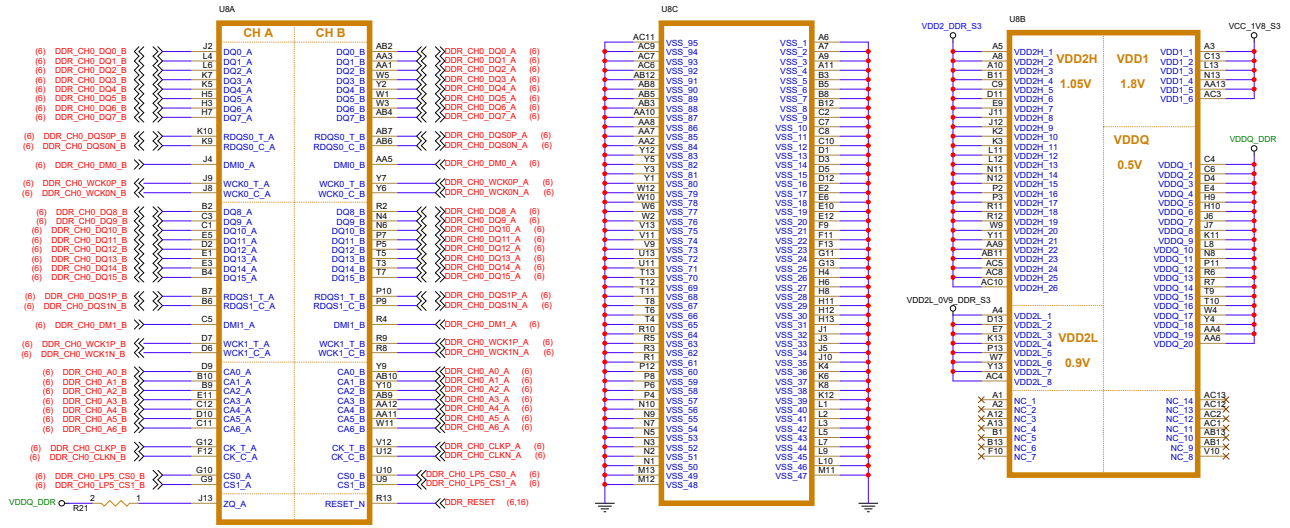


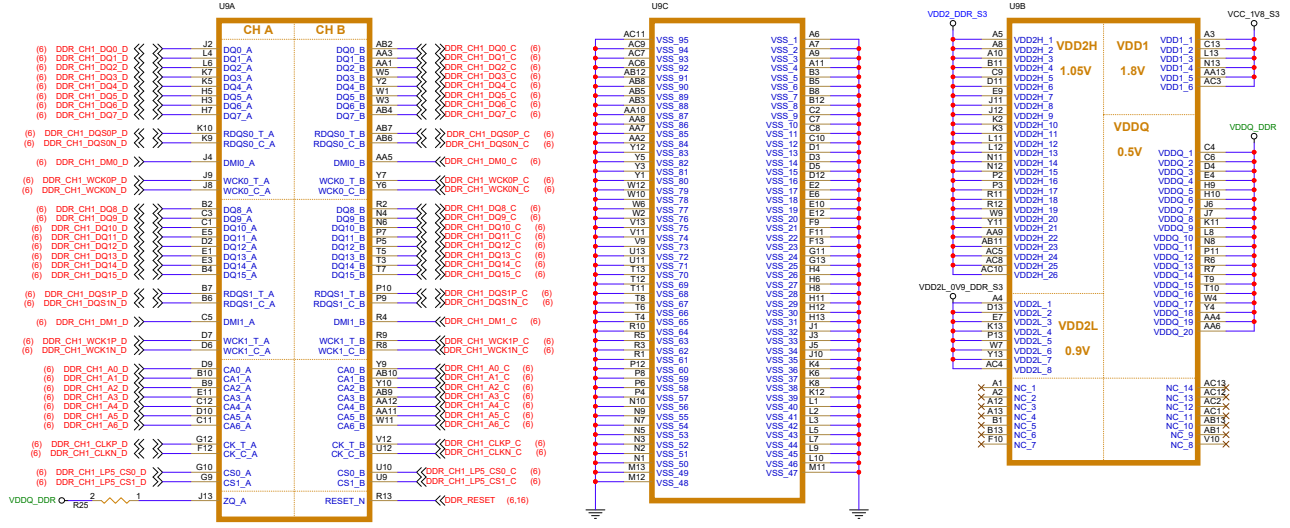


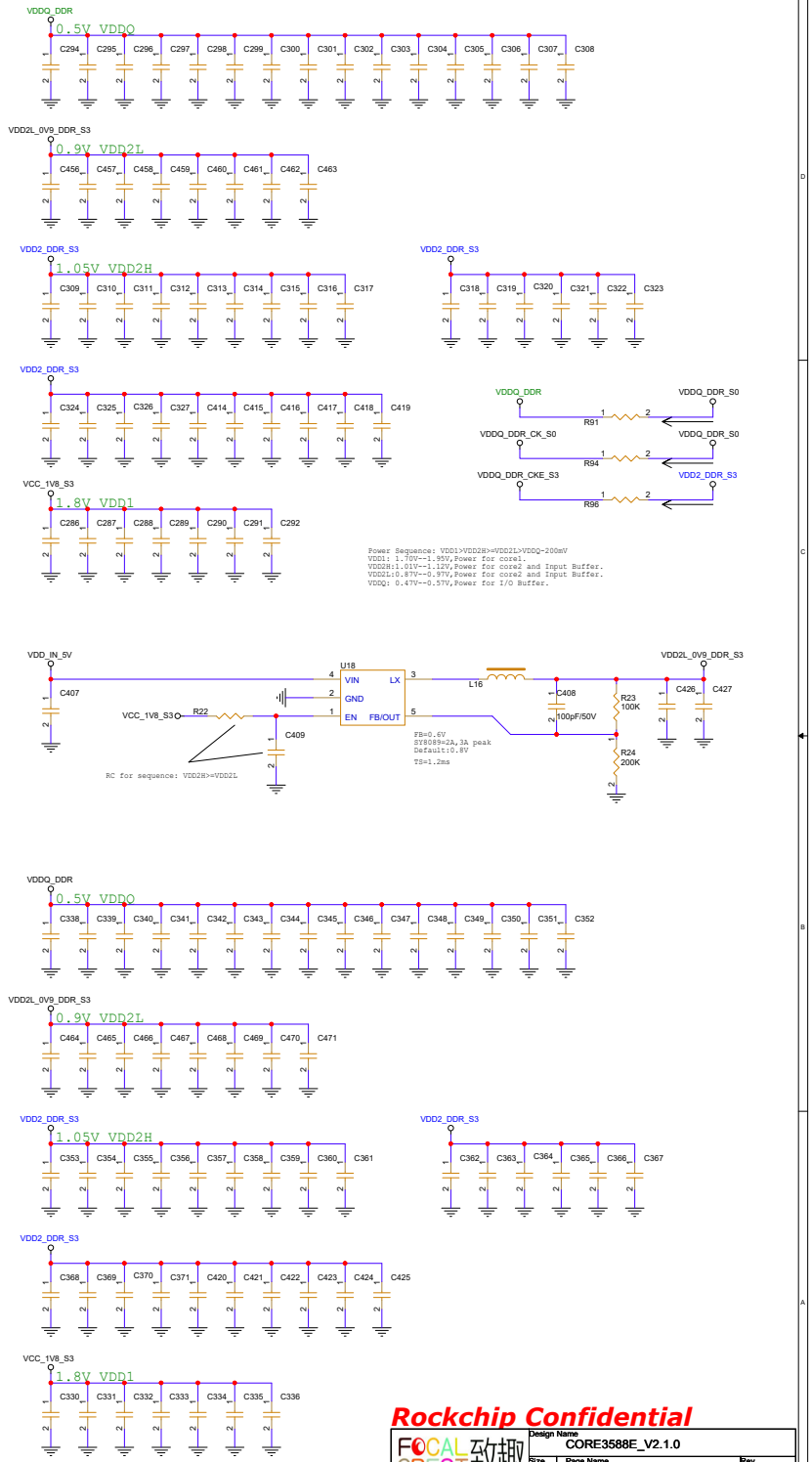
FOCAL CREST 致趣

Design Name	CORE3588E_V2.1.0	
Size A3	Page Name 15.Power_Ext Discrete	Rev V2.1.0
Date:	Sheet 15 of 20	

LPDDR5



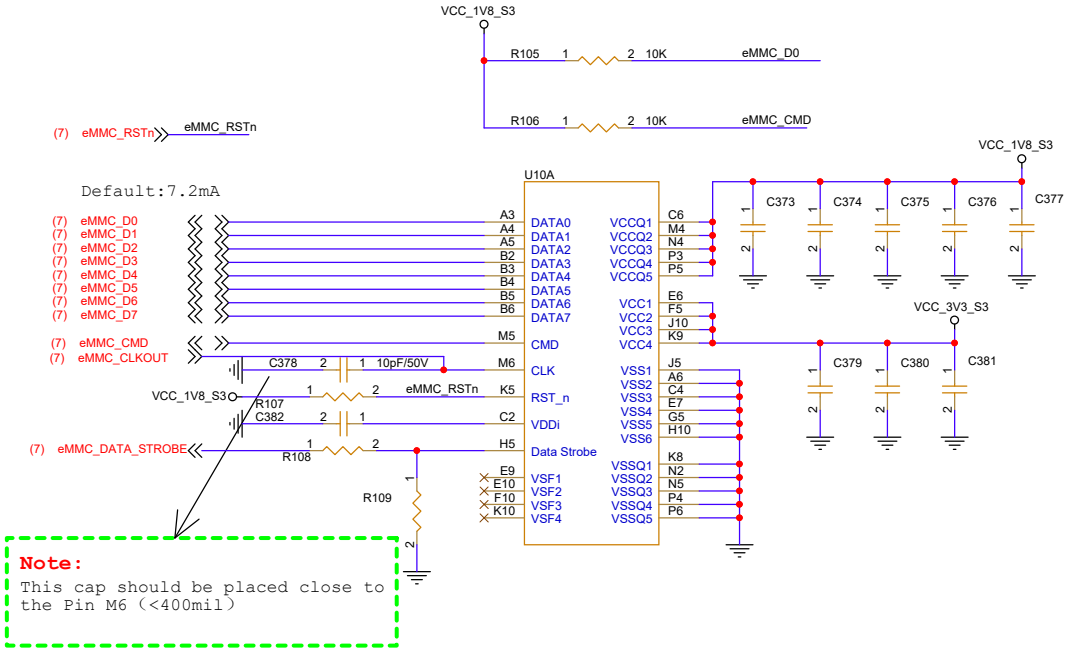


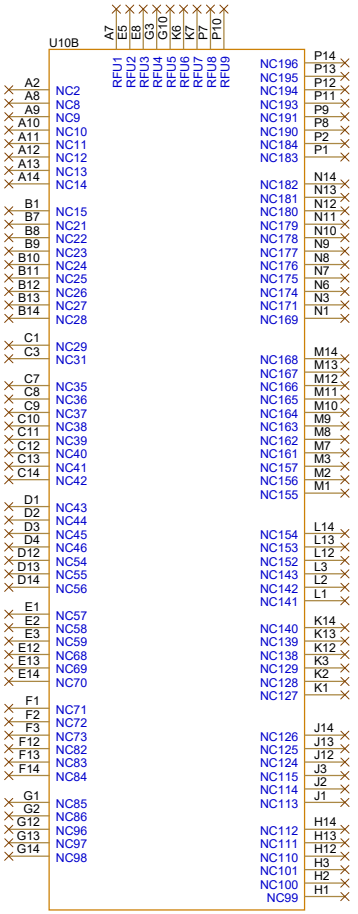


Rockchip Confidential

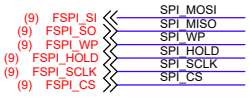
Design Name	CORE3588E_V2.1.0
Size A2	Page Name 16.DRAM-LPDDR5_246P_2X32bit
Rev	V2.1.0
Date:	Sheet 16 of 20

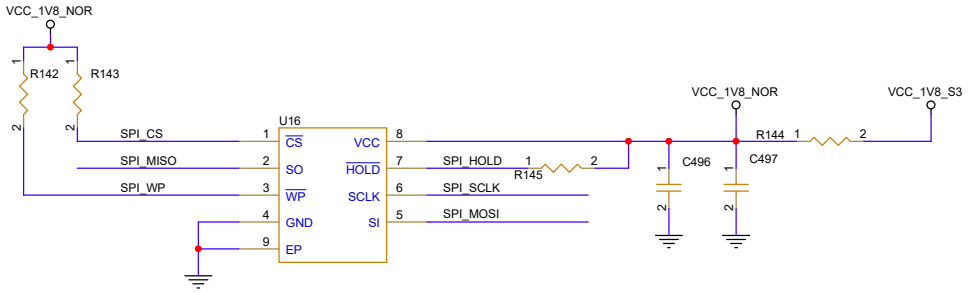
eMMC FLASH





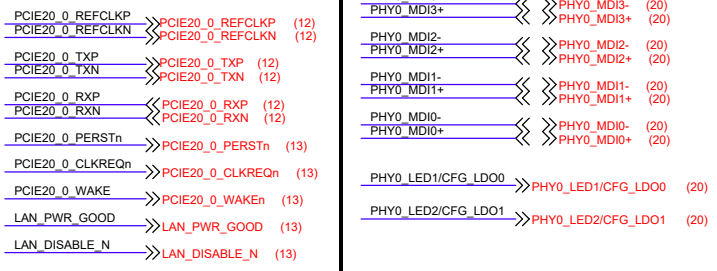
SPI NOR FLASH

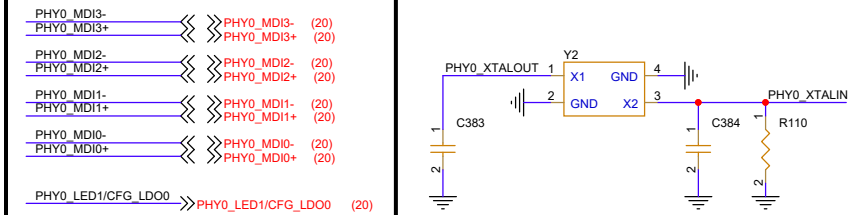


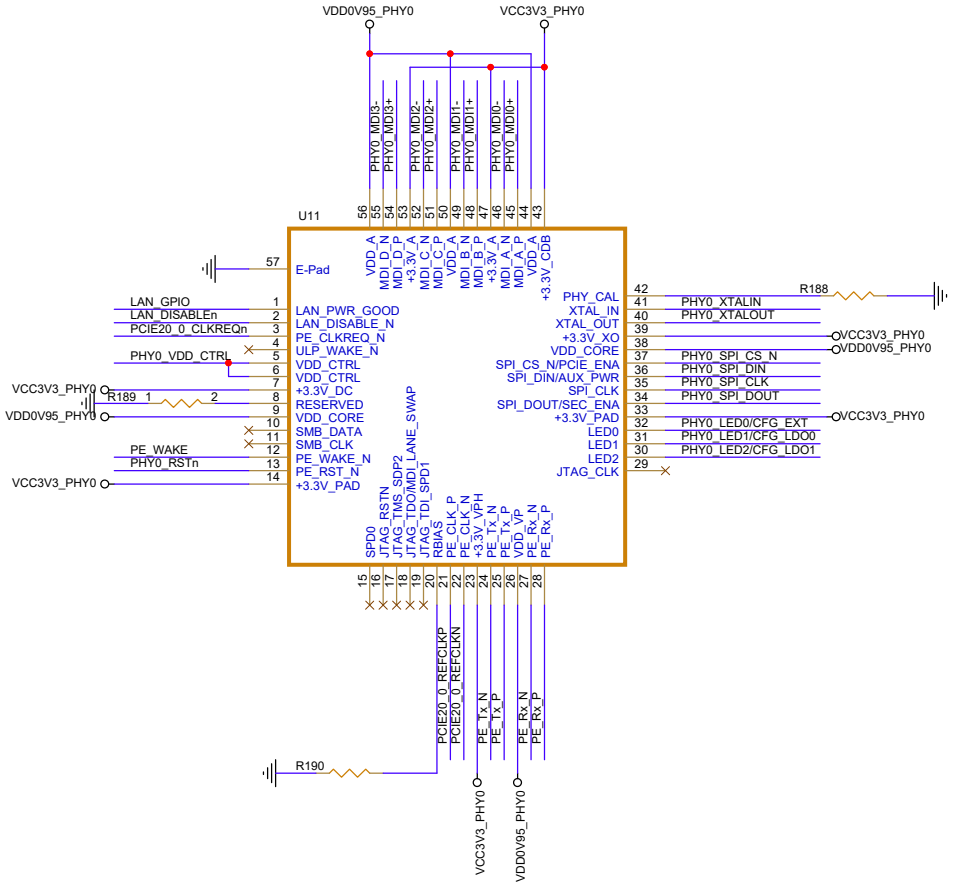


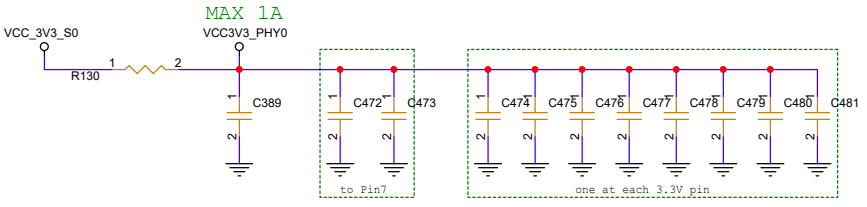
FOCAL CREST 致趣	Design Name: CORE3588E_V2.1.0	
	Size: A3 / Page Name: 17.Flash-eMMC/NOR-Flash	Rev: V2.1.0
	Date:	Sheet 17 of 20

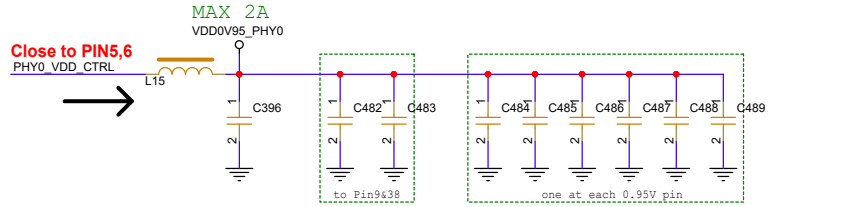
RGMII TO RJ45

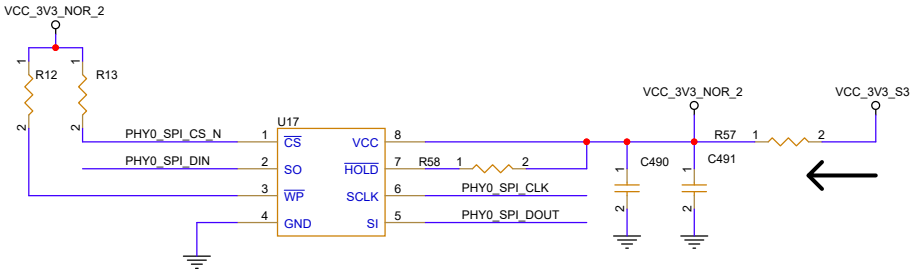


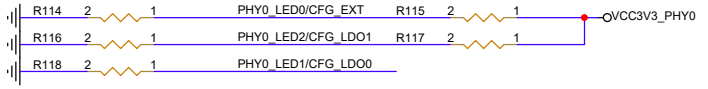


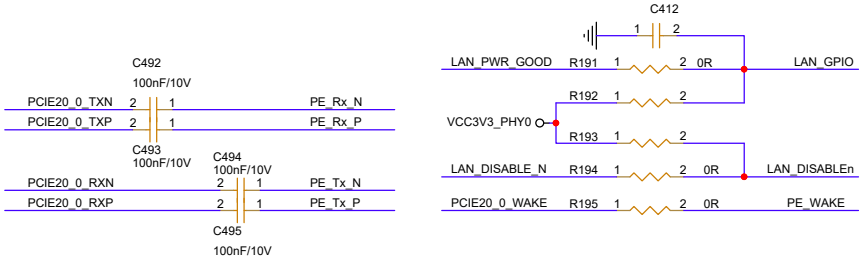


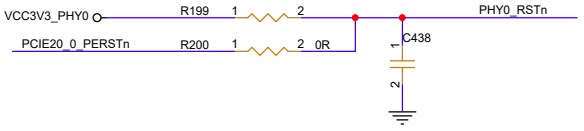










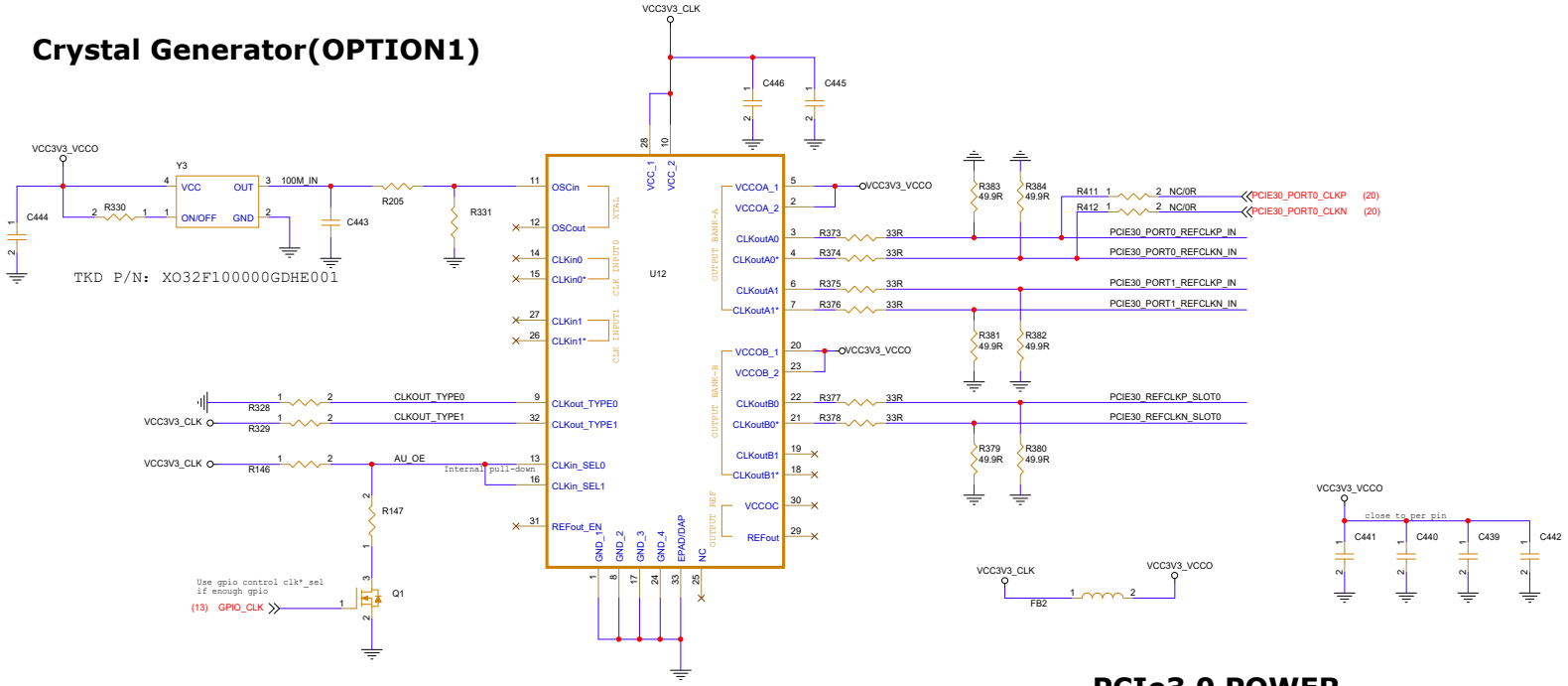


FOCAL CREST 致趣

Design Name	CORE3588E_V2.1.0
Size A3 / Page Name	18.Ethernet-I226V
Rev	V2.1.0
Date: / Sheet	18 of 20

PCIE30_PORT0_REFCLKP_IN (12)
PCIE30_PORT0_REFCLKN_IN (12)
PCIE30_PORT1_REFCLKP_IN (12)
PCIE30_PORT1_REFCLKN_IN (12)
PCIE30_REFCLKP_SLOT0 (20)
PCIE30_REFCLKN_SLOT0 (20)
PCIE_PWREN_H (13)

Crystal Generator(OPTION1)



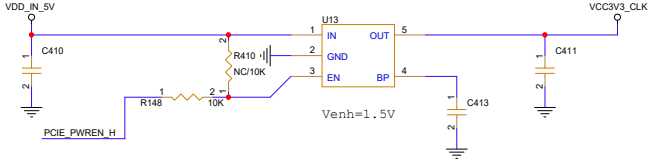
CLKIN SELECT

CLKIN_SEL1	CLKIN_SEL0	CLK Buffer Type
0	0	CLKIN0
0	1	CLKIN1
1	0	CRYSTAL or AC MODE
1	1	CRYSTAL DC MODE

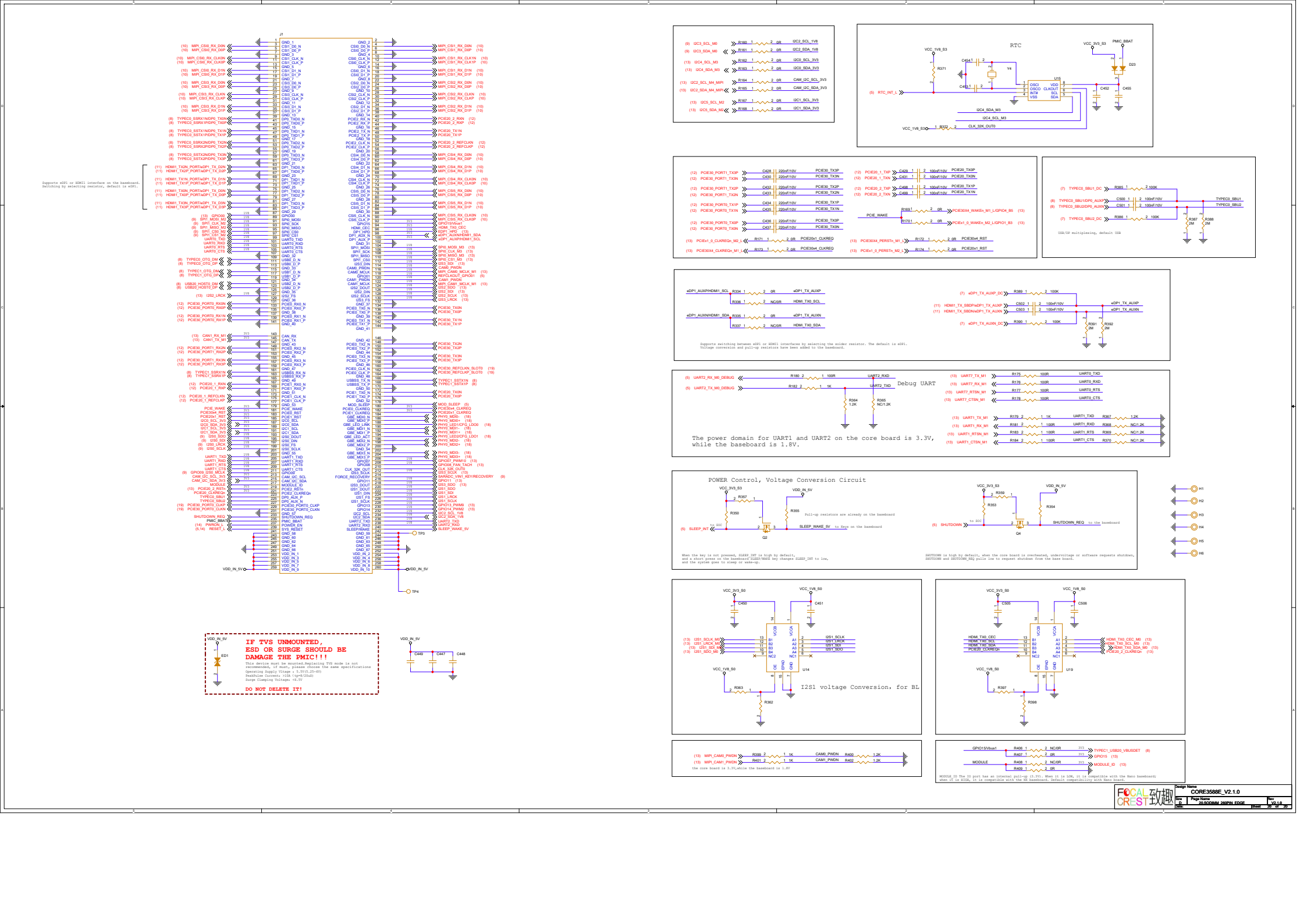
CLKOUT TYPE SELECT

CLKOUT_TYPE1	CLKOUT_TYPE0	CLK Buffer Type
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	HIZ

PCIe3.0 POWER



Design Name	CORE3588E_V2.1.0	
Size: C	Page Name: 19.PCIE-PCIE3.0 CLK GENERATOR	Rev: V2.1.0
Date:	Sheet: 19 of 20	



J1
Supports eDP1 or HDMI1 interface on the baseboard. Switching by selecting resistor, default is eDP1.
RTC
Supports switching between eDP1 or HDMI1 interfaces by selecting the solder resistor. The default is eDP1. Voltage conversion and pull-up resistors have been added to the baseboard.
Debug UART
The power domain for UART1 and UART2 on the core board is 3.3V, while the baseboard is 1.8V.
POWER Control, Voltage Conversion Circuit
Pull-up resistors are already on the baseboard
When the key is not pressed, SLEEP_INT is high by default, and a short press on the baseboard SLEEP/WAKE key changes SLEEP_INT to low, and the system goes to sleep or wake-up.
SHUTDOWN is high by default, when the core board is overheated, undervoltage or software requests shutdown, SHUTDOWN and SHUTDOWN_REQ pulls low to request shutdown from the base board.
I2S1 voltage Conversion, for BL
the core board is 3.3V,while the baseboard is 1.8V
MODULE_ID The IO port has an internal pull-up (3.3V). When it is LOW, it is compatible with the Nano baseboard; when it is HIGH, it is compatible with the NX baseboard. Default compatibility with Nano board.
IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!
This device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Vltage = 5.5V(5.25-6V)
Peak Pulse Current= 112A (tp=8/20uS)
Surge Clamping Voltage= 46.5V
DO NOT DELETE IT!
FOCAL CREST 致趣
Design Name CORE3588E_V2.1.0
Size D
Page Name 20.5CDIMM 260PIN EDGE
Rev V2.1.0
Date:
Sheet 20 of 20